

FIG. 1

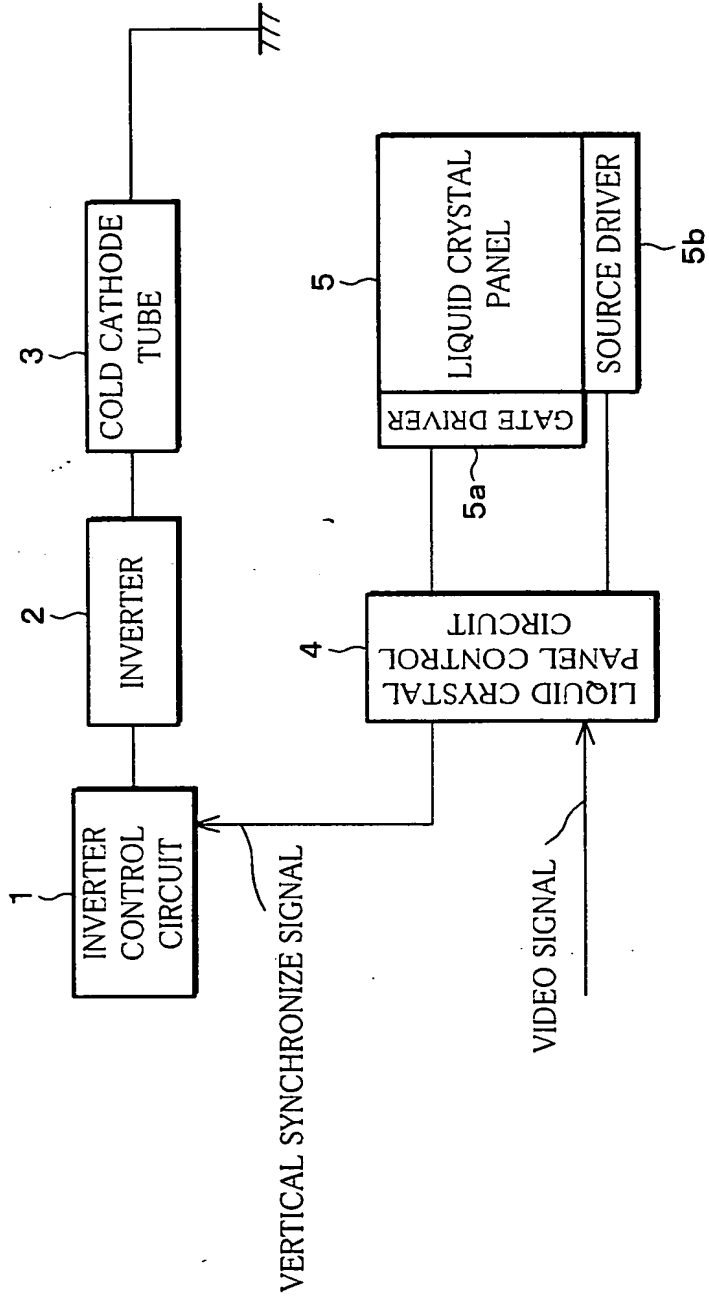
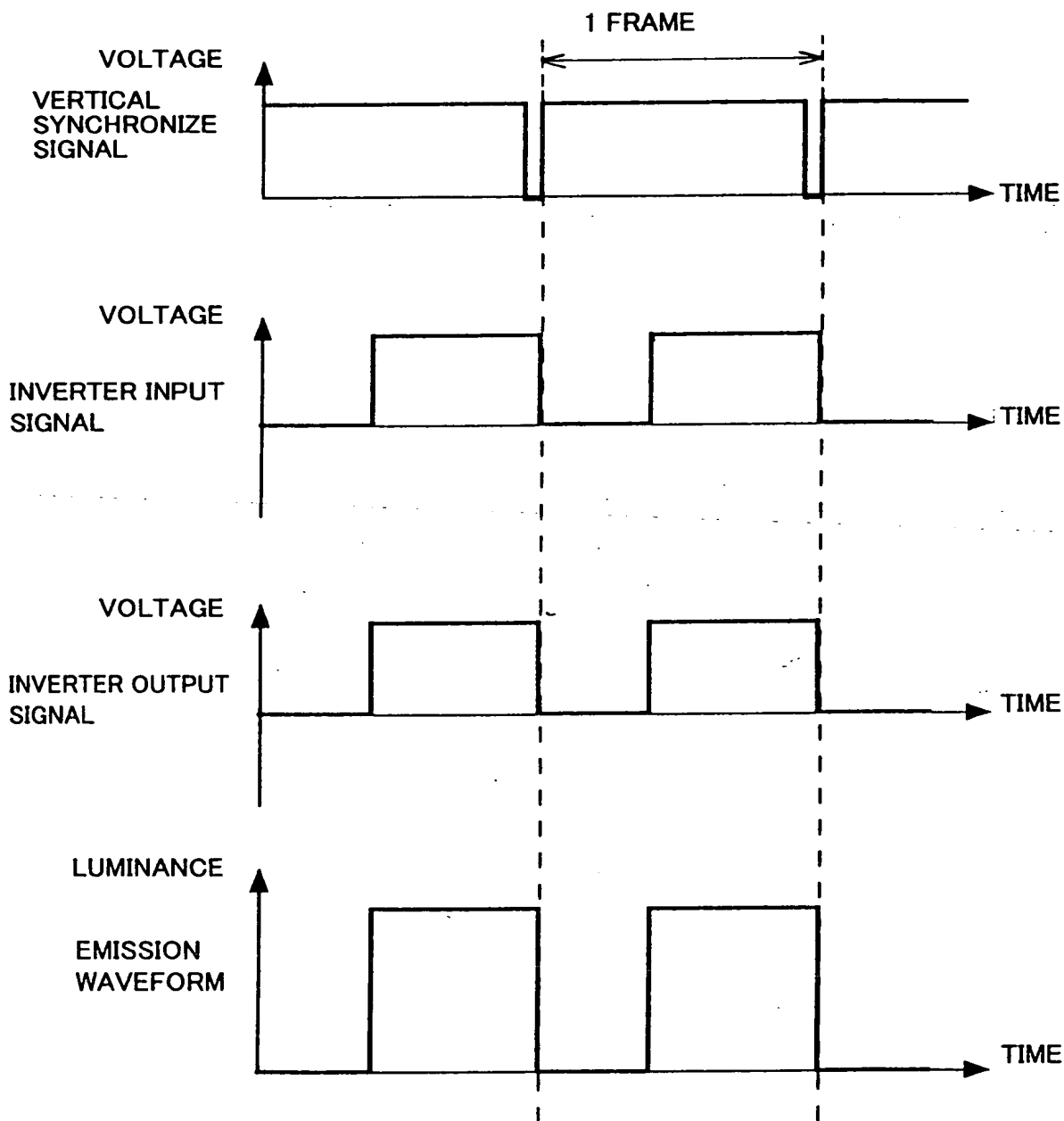
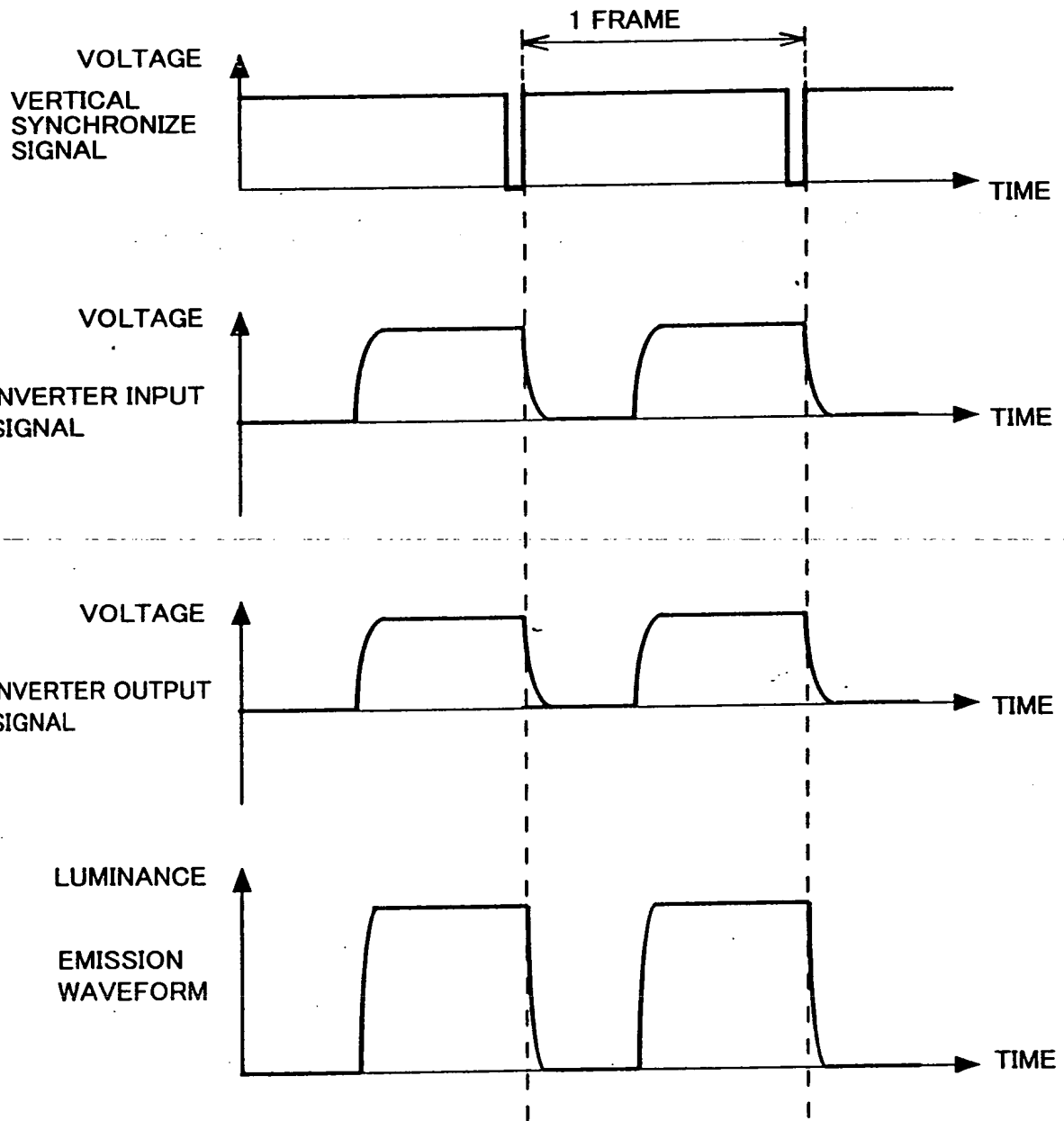


FIG. 2



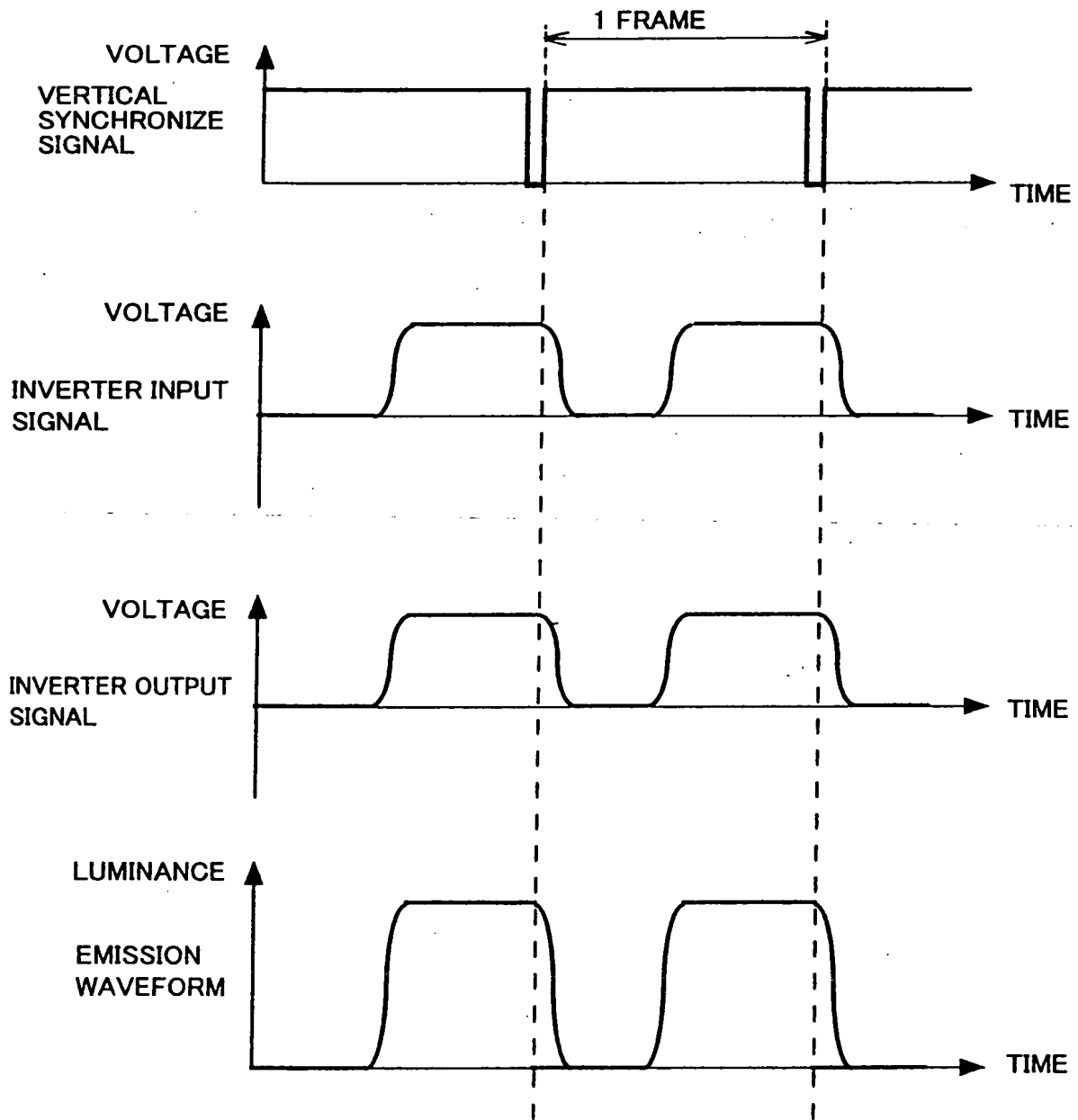
10281-10100

F I G . 3



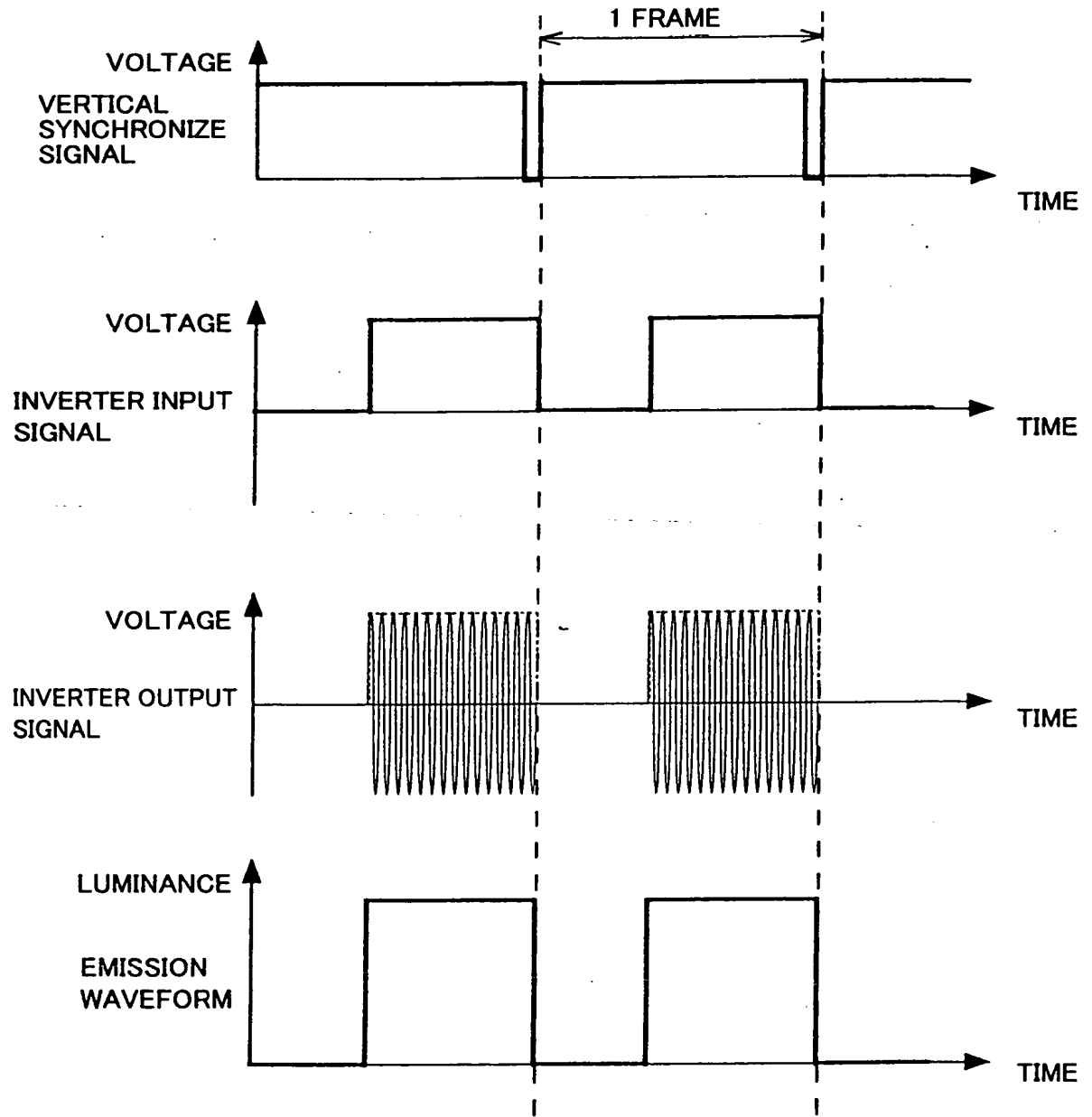
4 3 2 1 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

FIG. 4



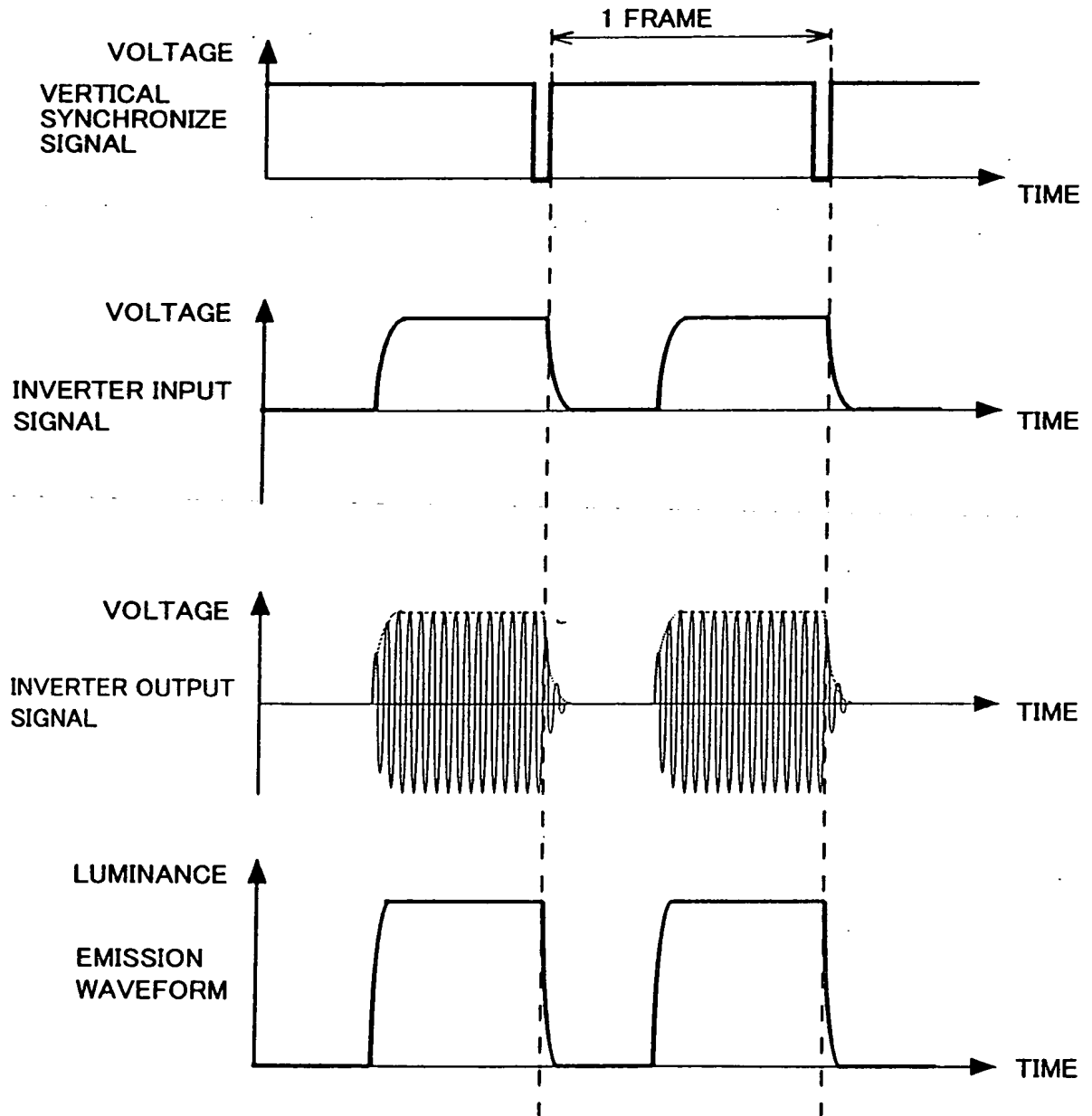
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FIG. 5



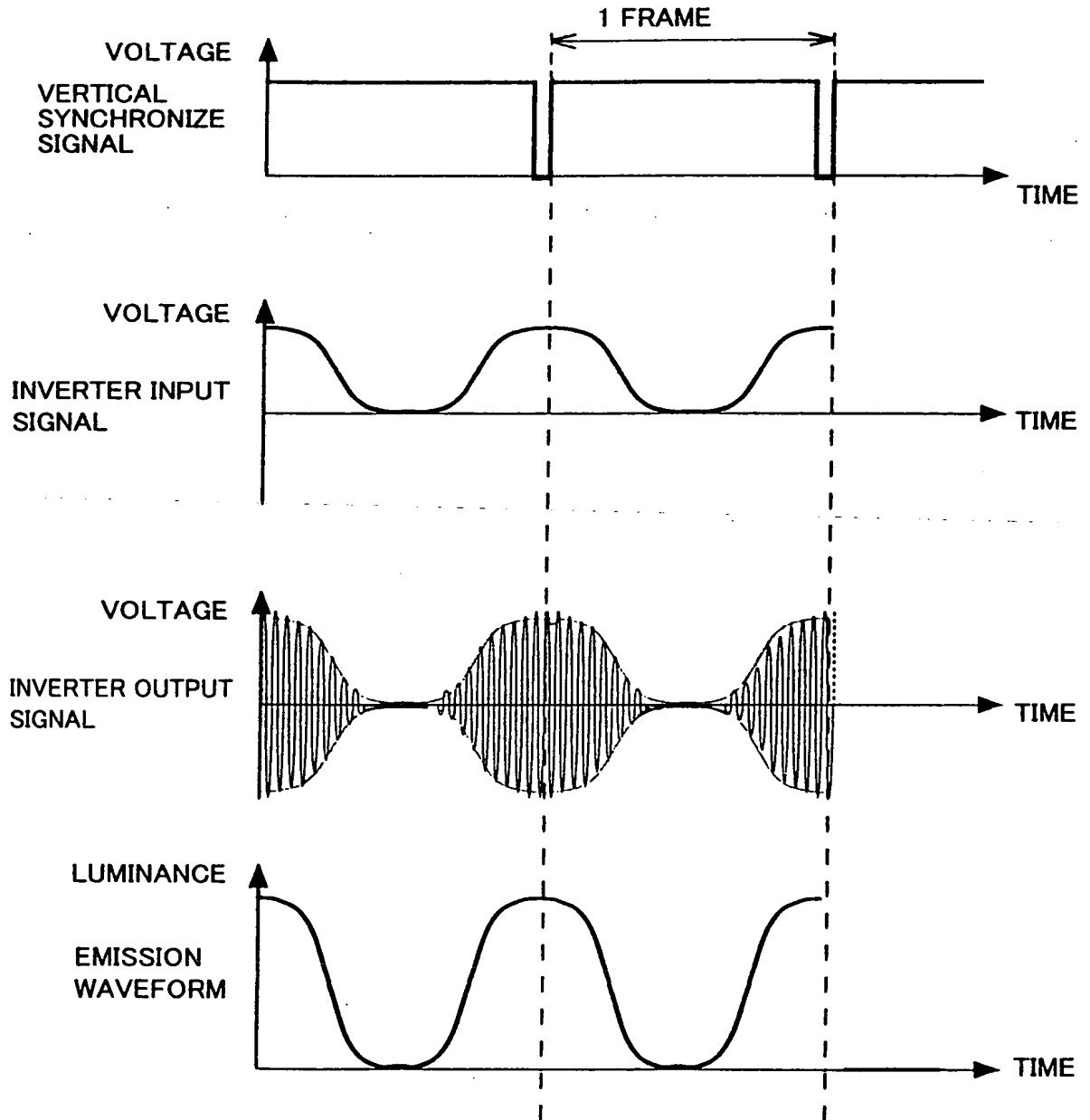
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FIG. 6



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FIG. 7



16 22 1 210 1 13 24 23 25 26 27 28 29 30

FIG. 8

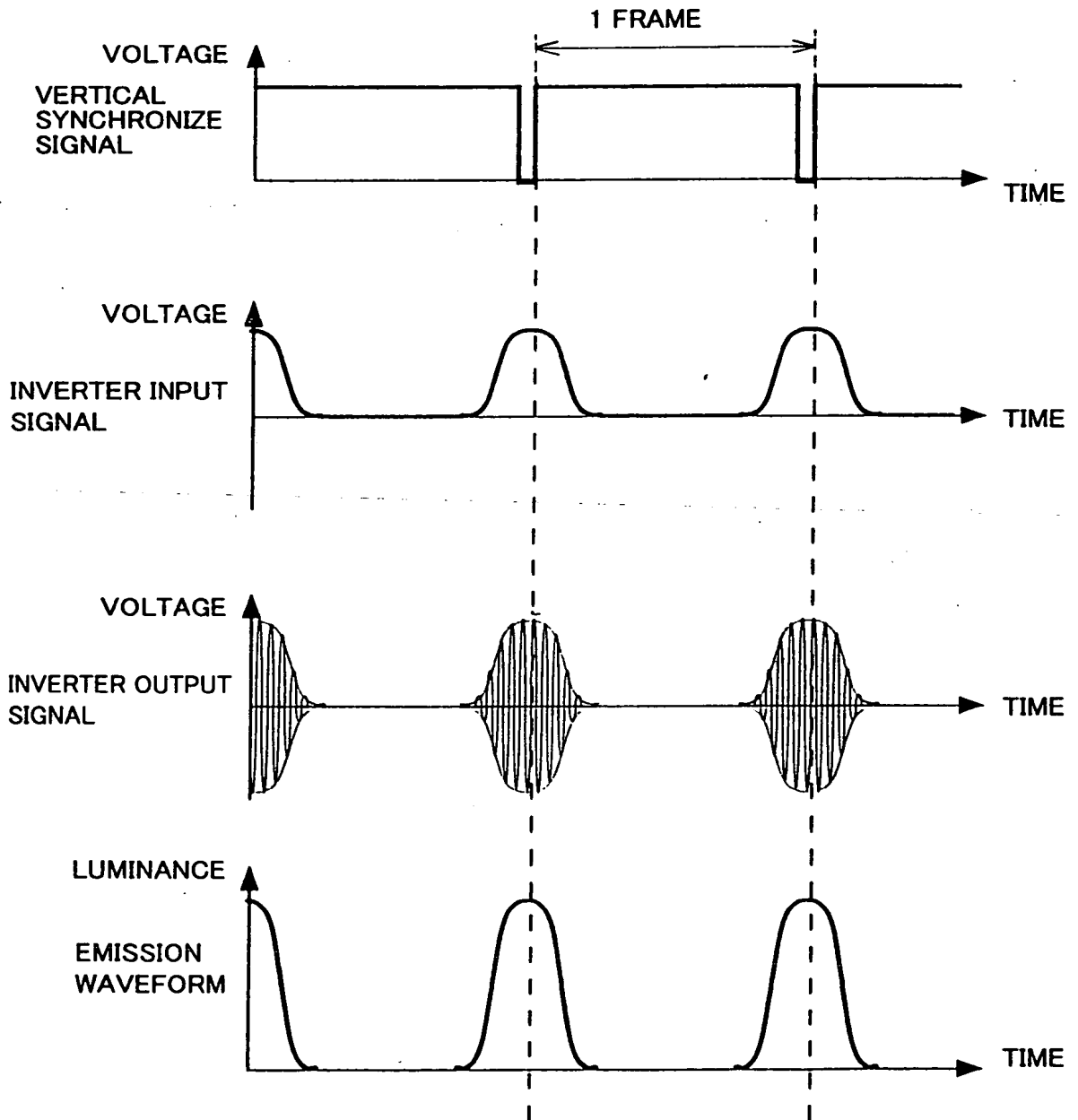


FIG. 9

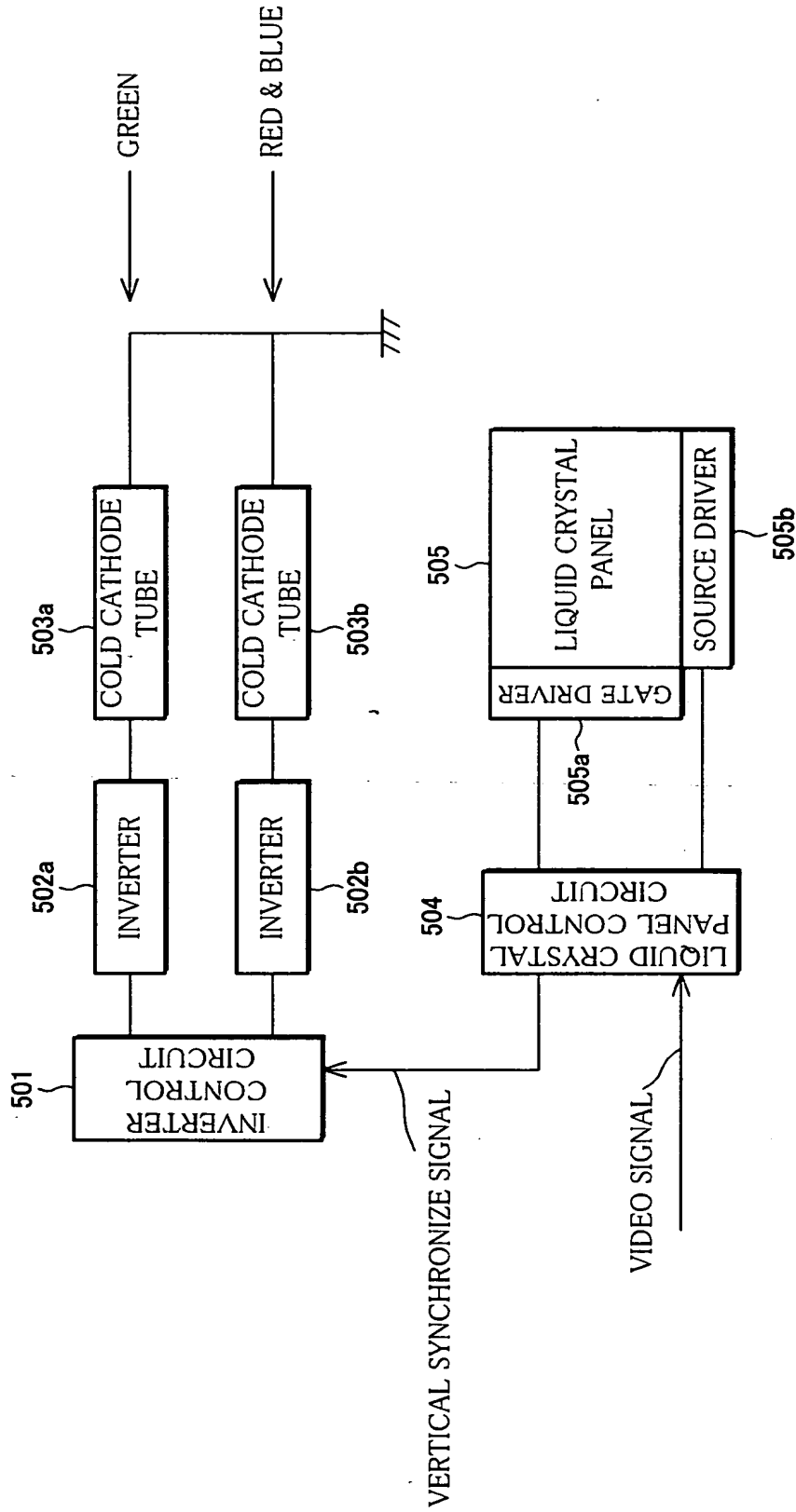


FIG. 10

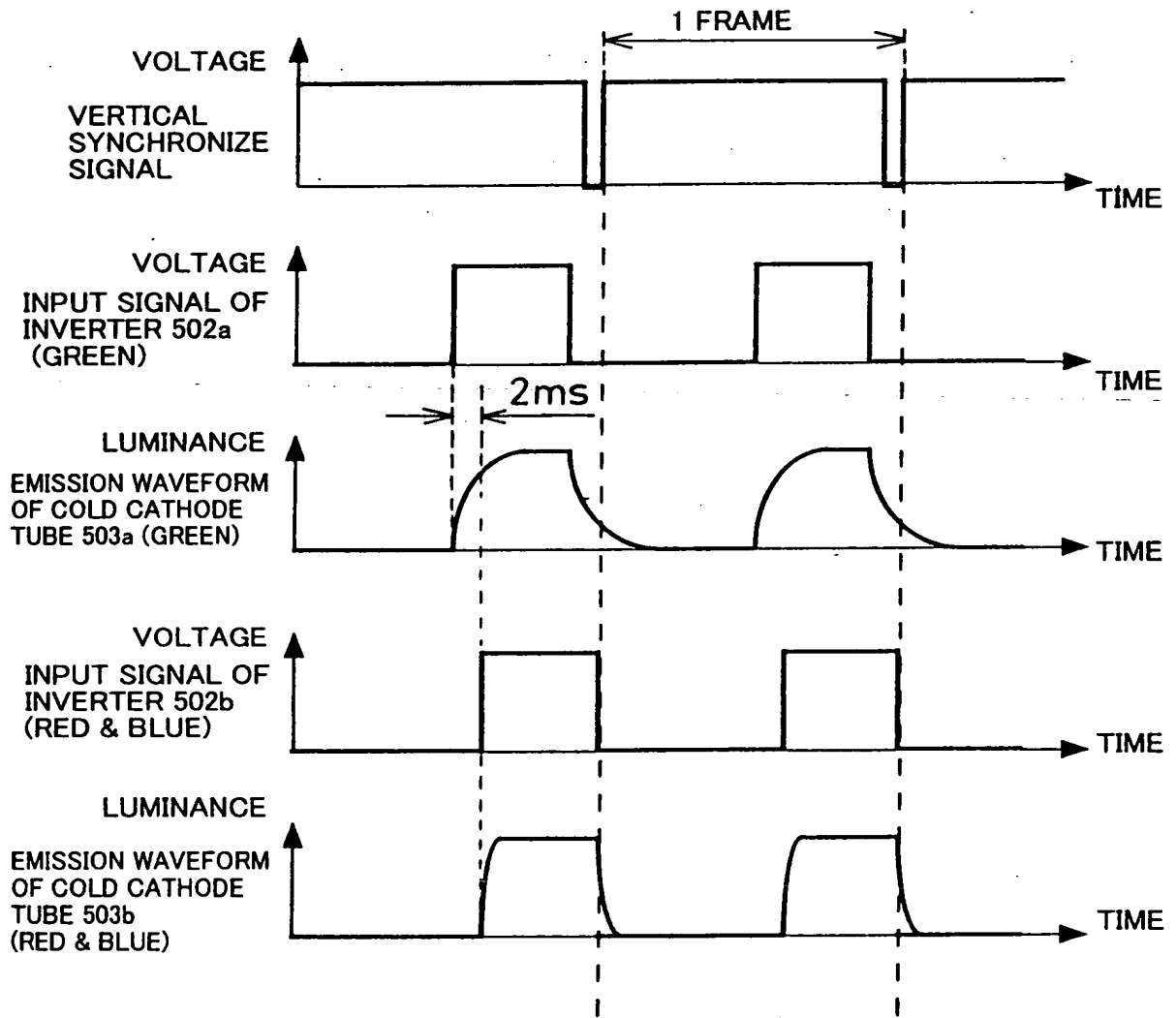


FIG. 10

FIG. 11

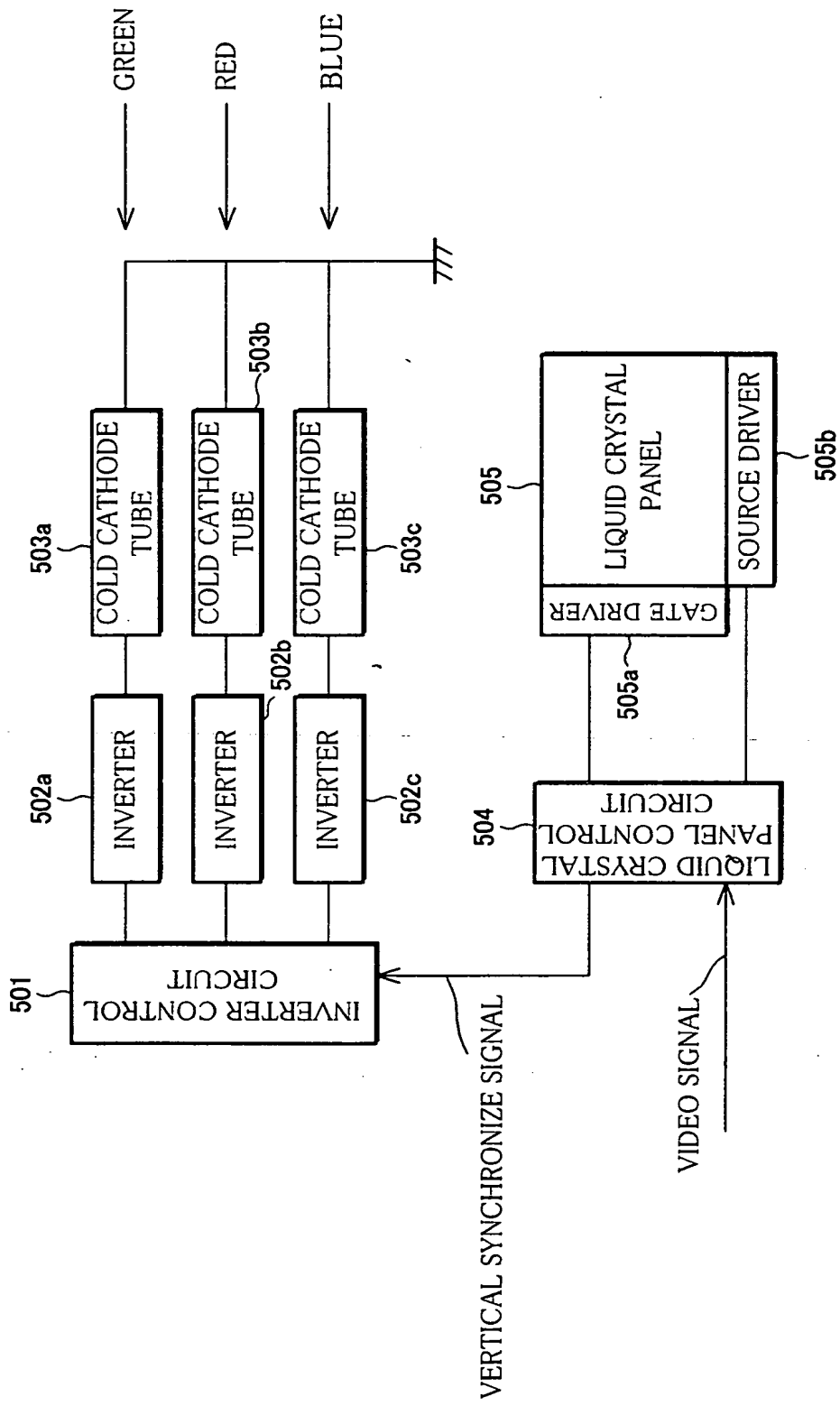
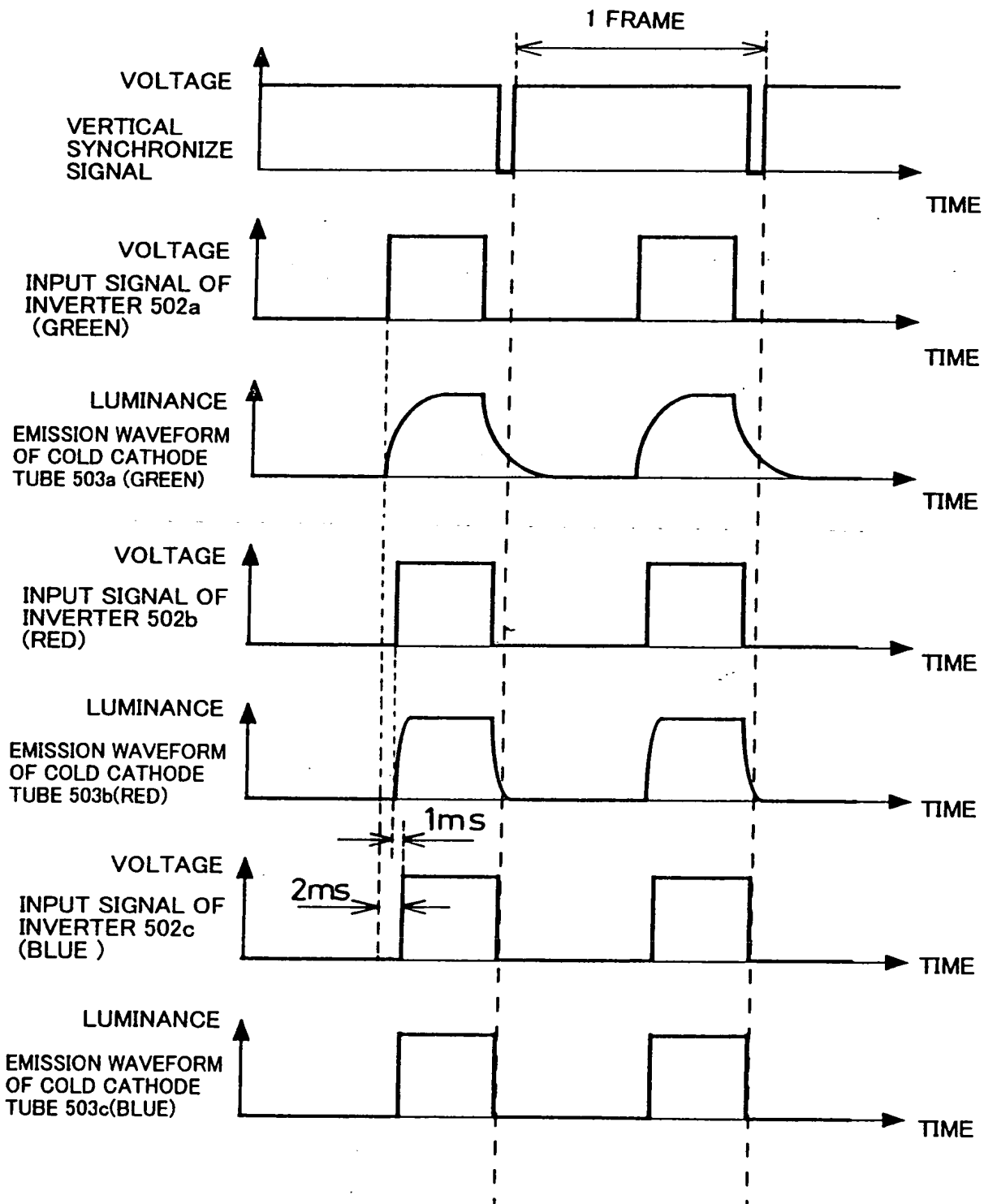


FIG. 12



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FIG. 13

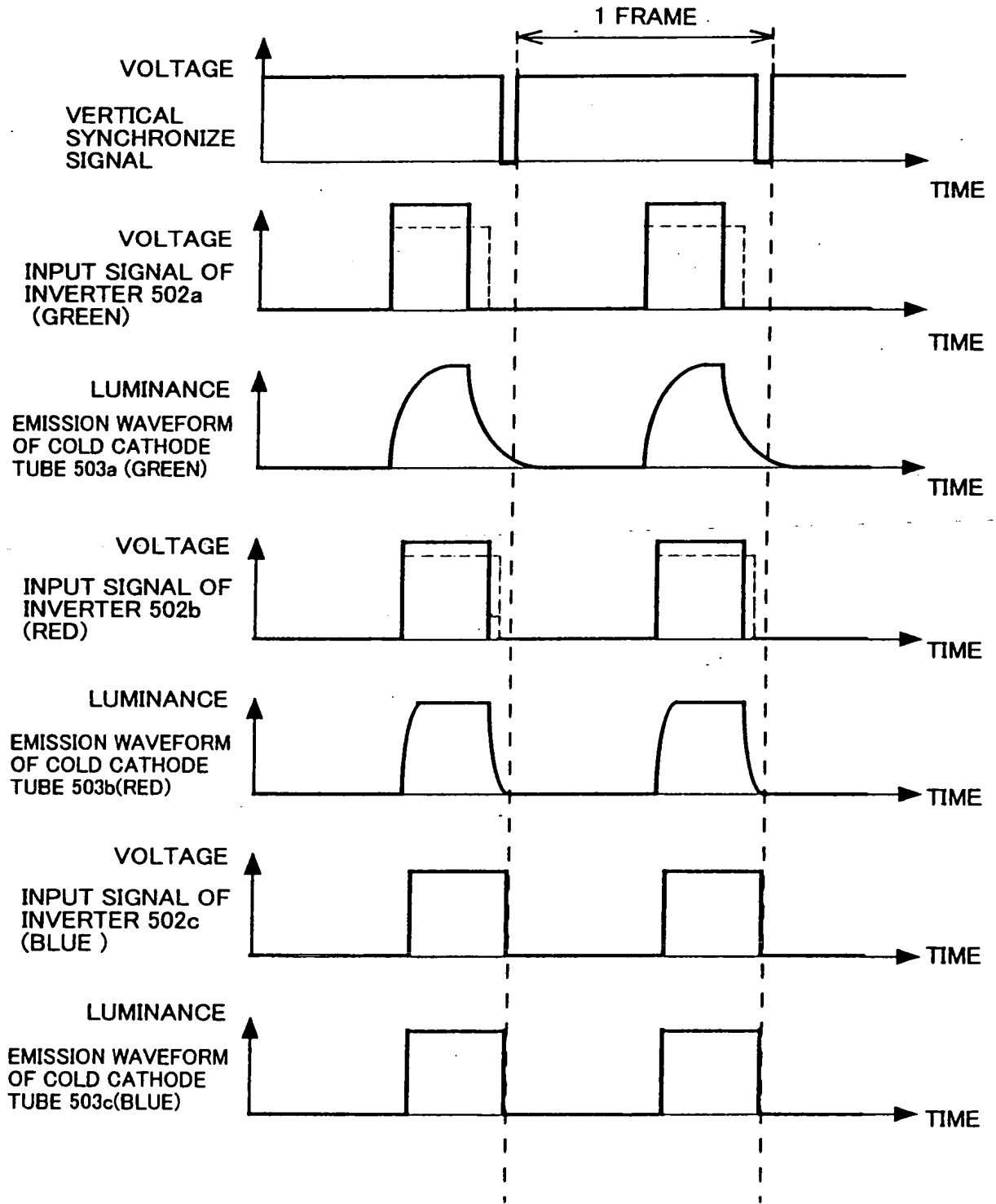


FIG. 14

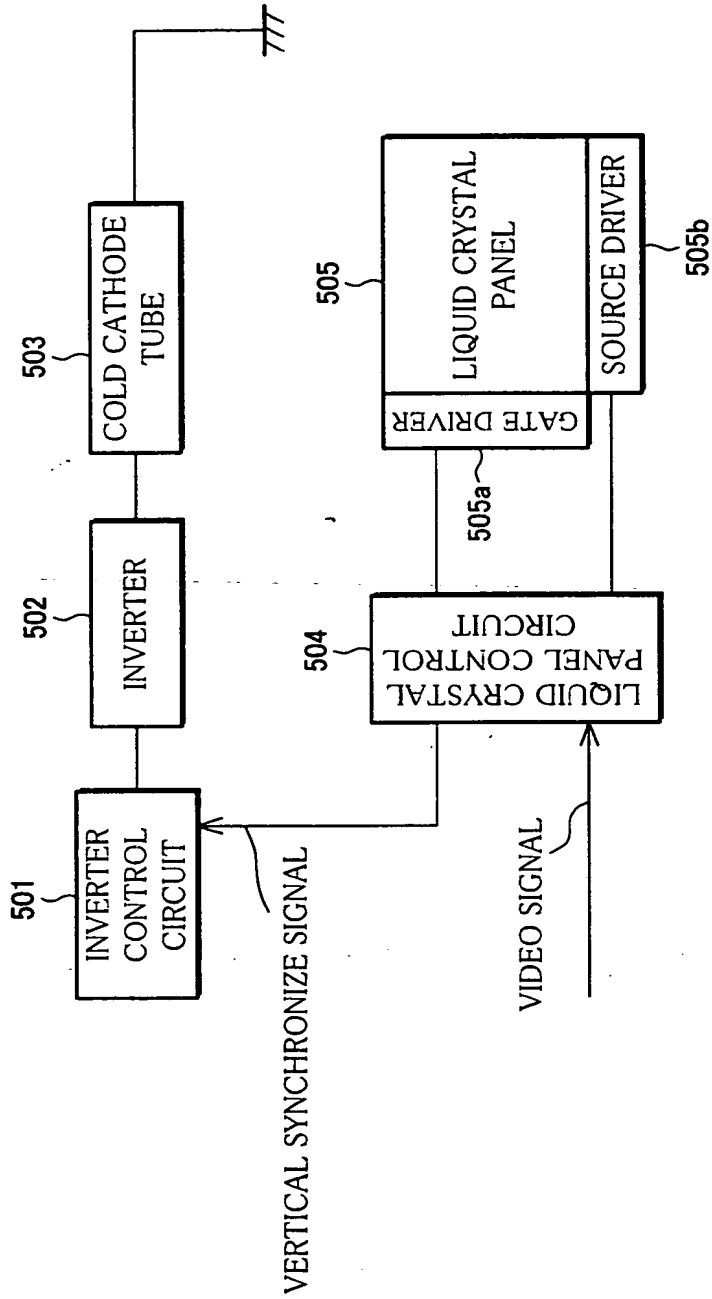
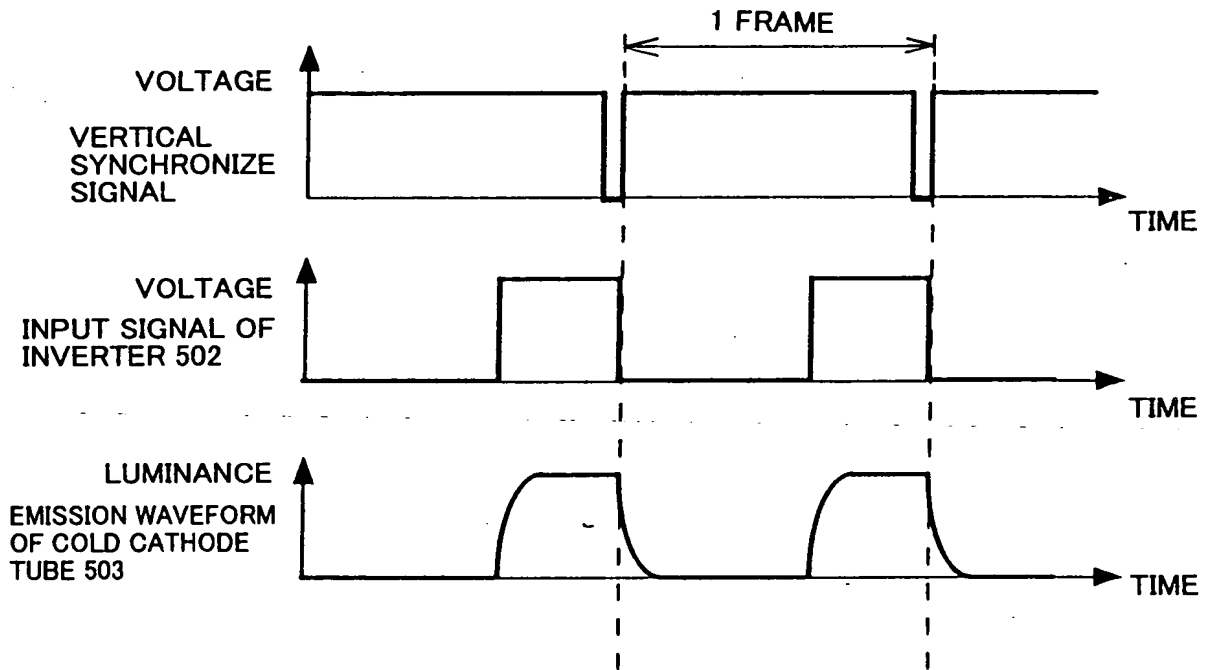
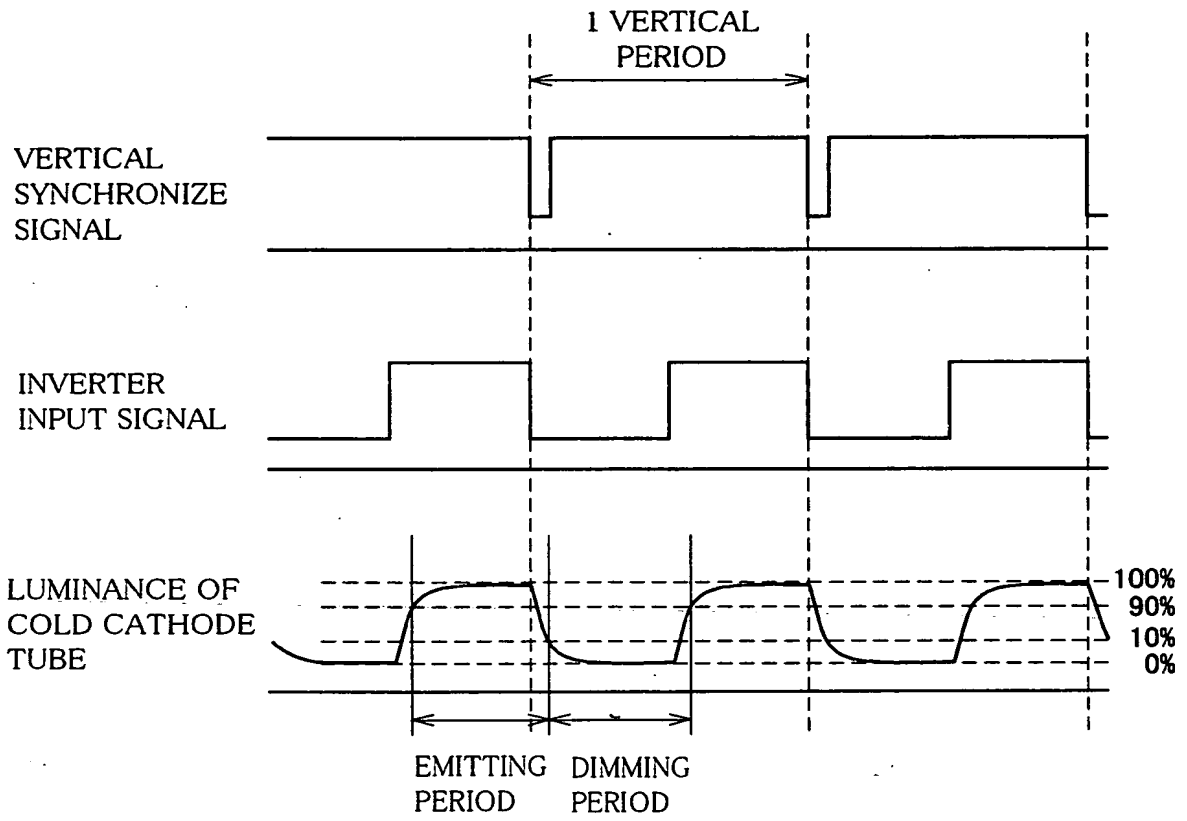


FIG. 15



TOP SECRET

FIG. 16



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FIG. 17

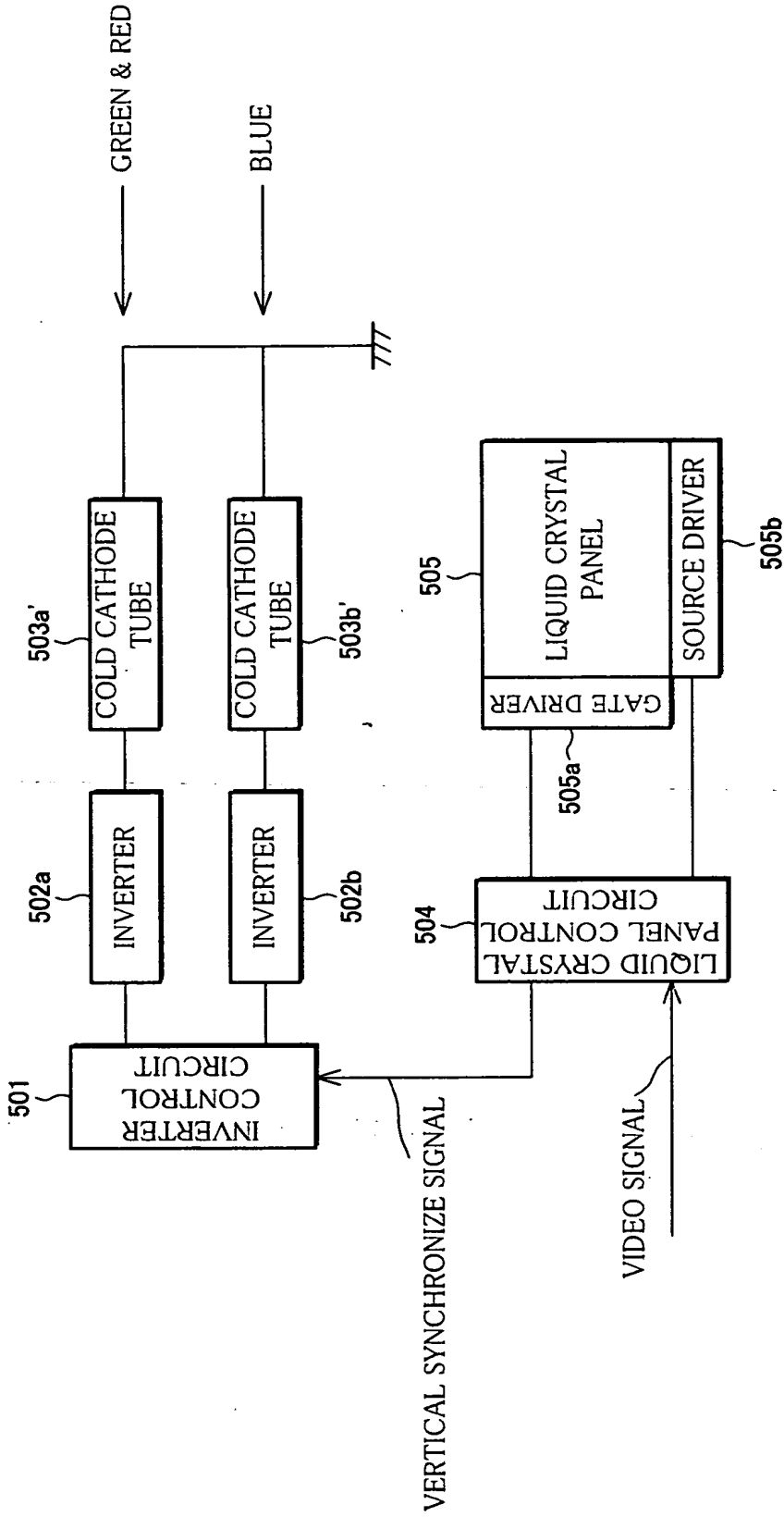
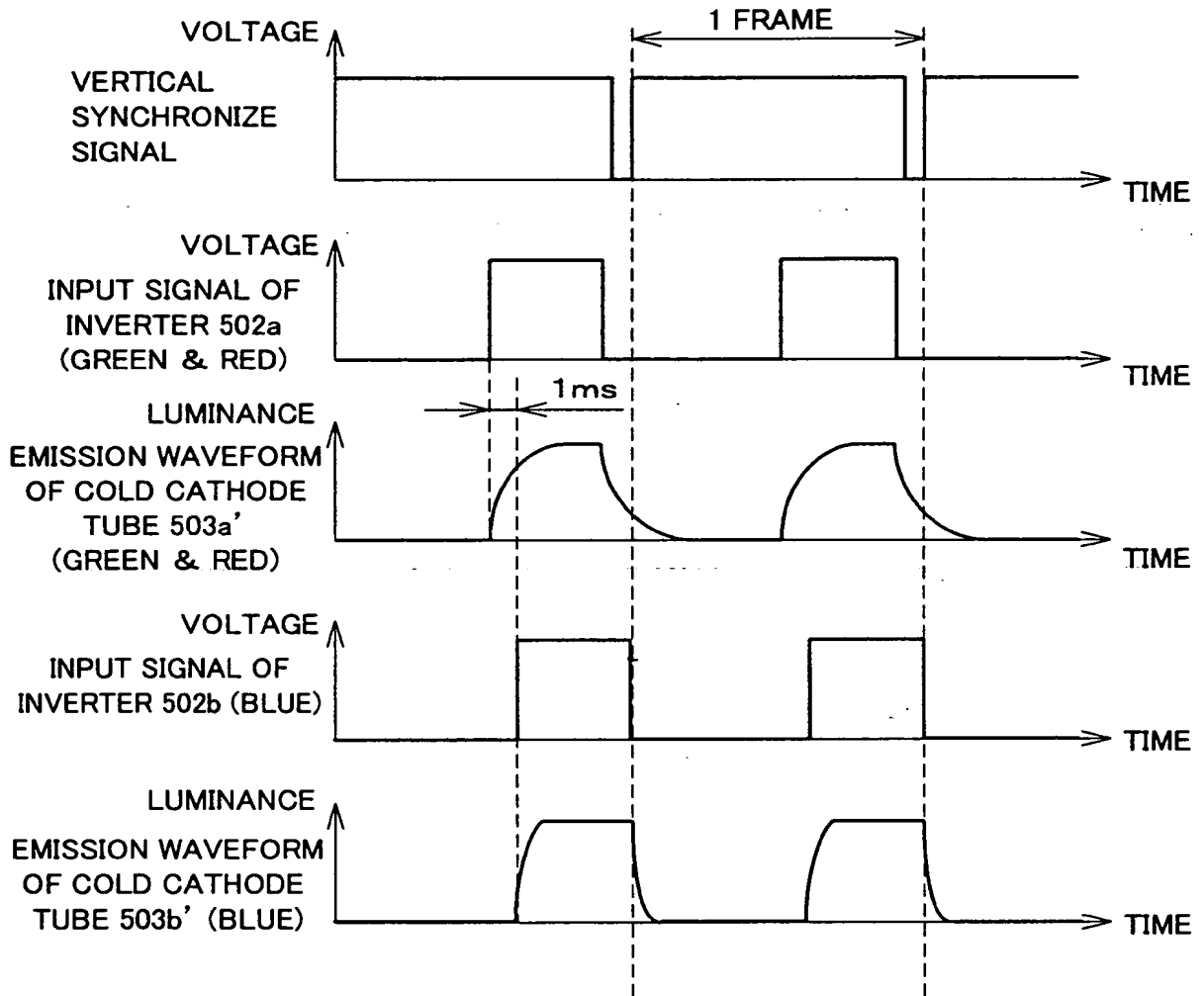
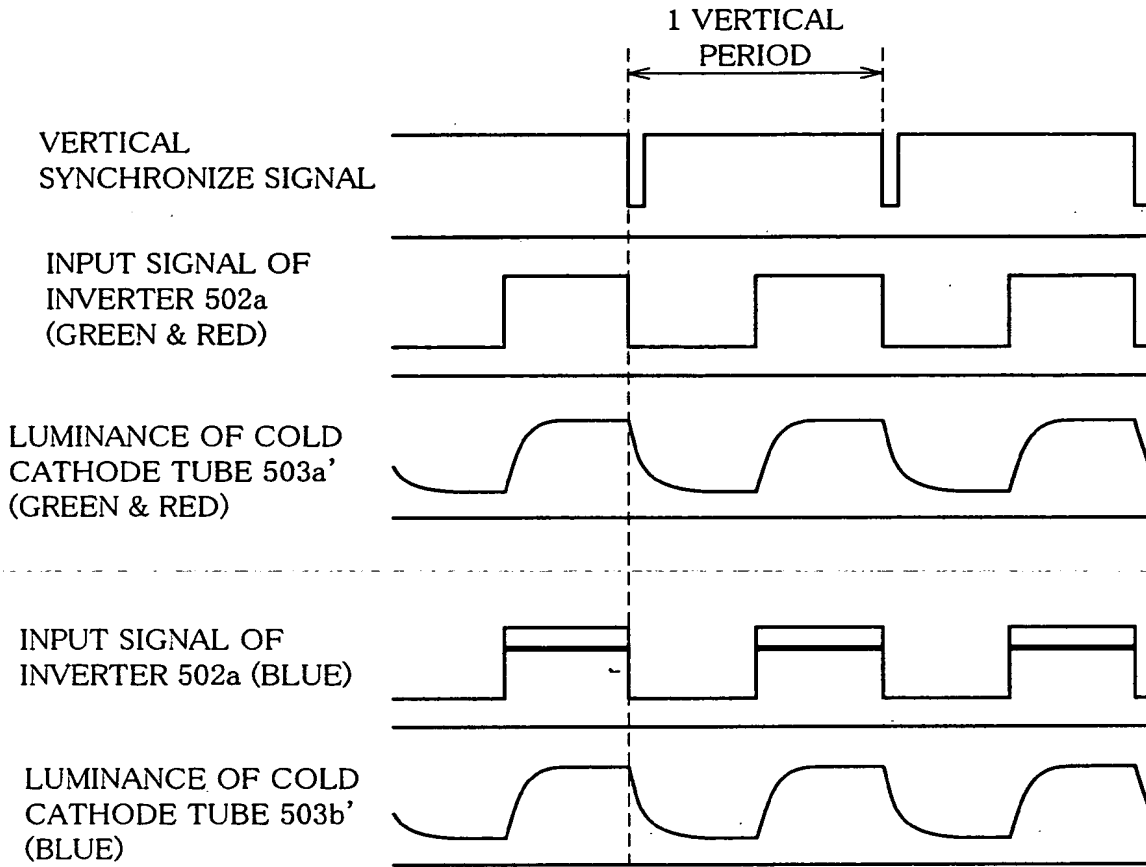


FIG. 18



409759-1-0000

FIG. 19



50352620

FIG. 20

BLOCK DIAGRAM OF ILLUMINATION DEVICE

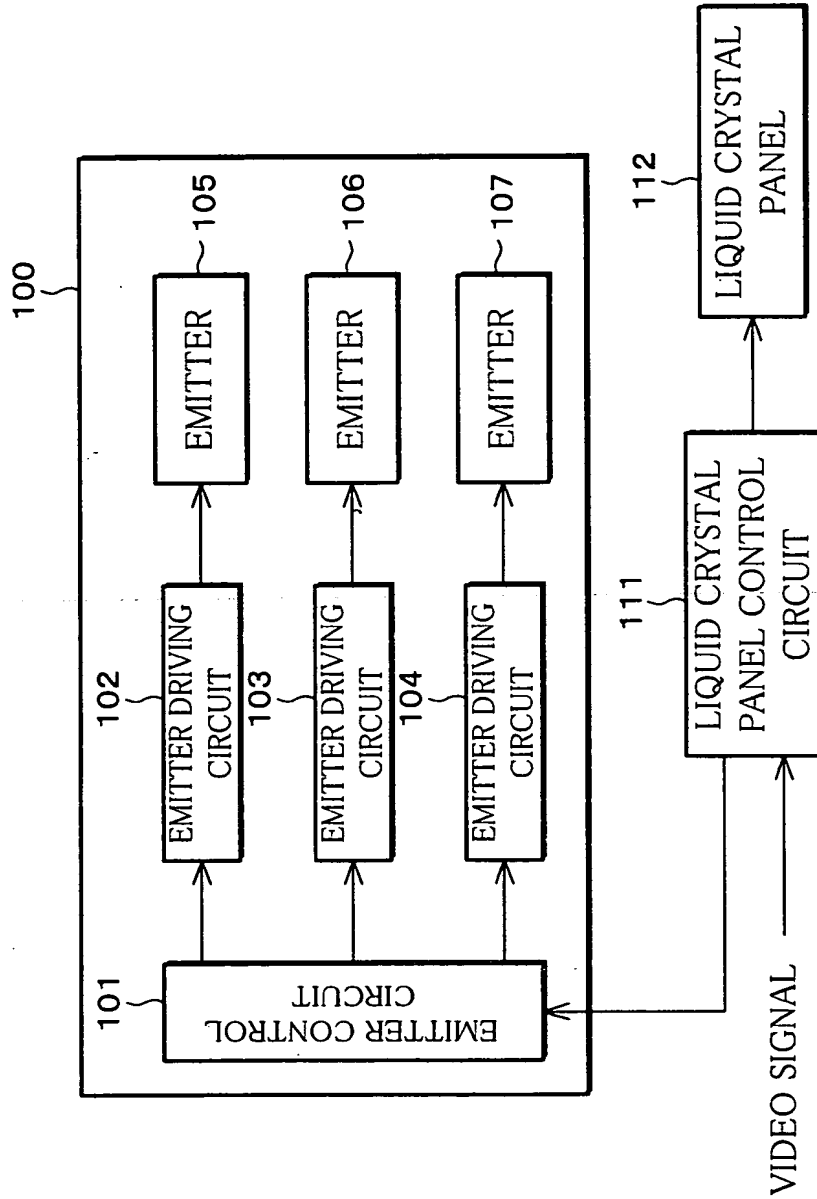
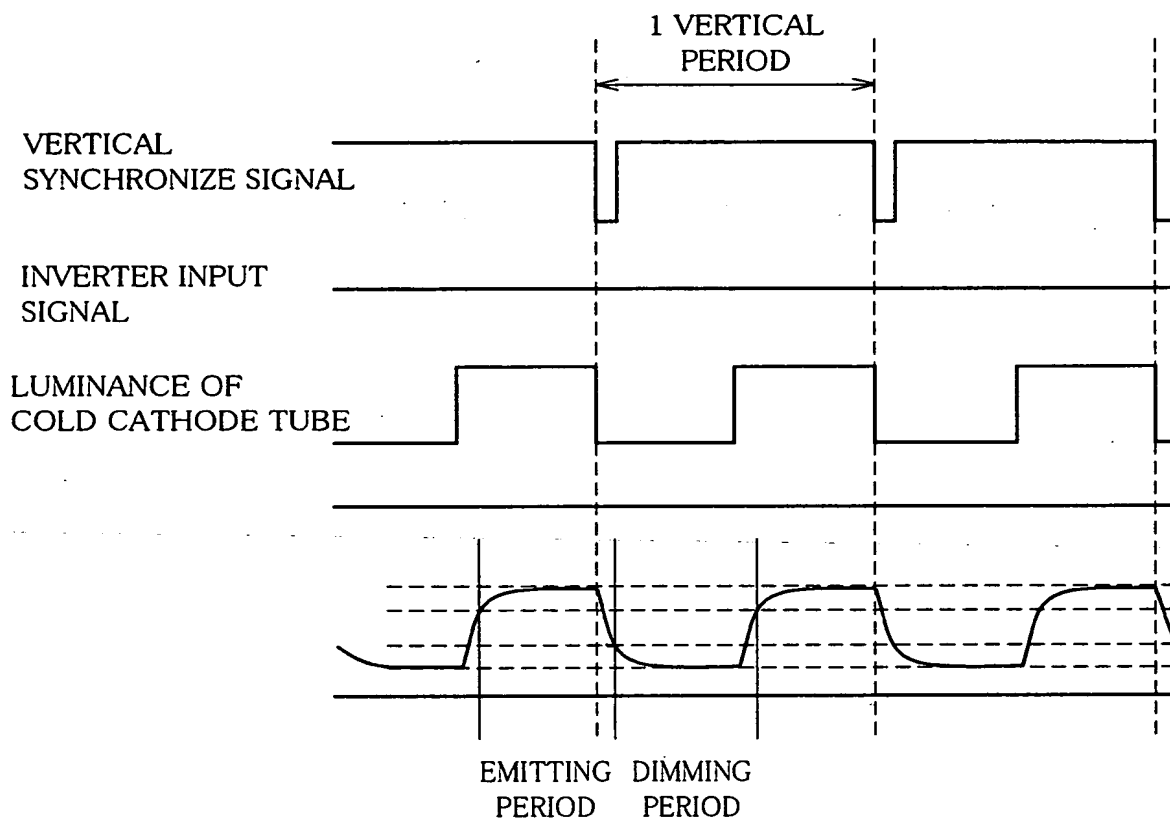
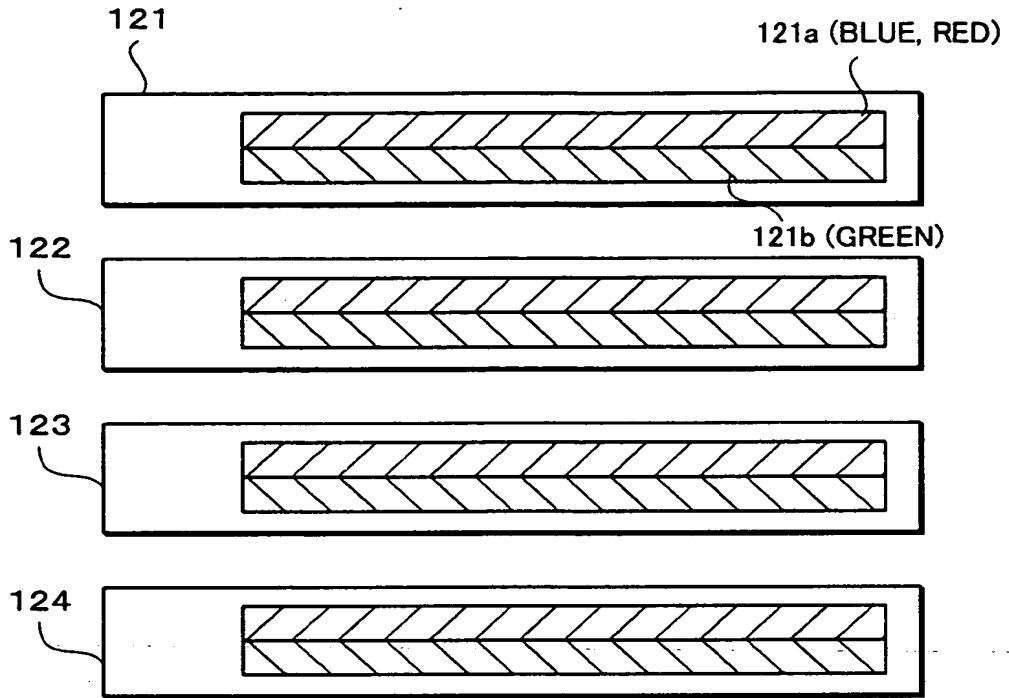


FIG. 21



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F I G. 2 2 (a)



F I G. 2 2 (b)

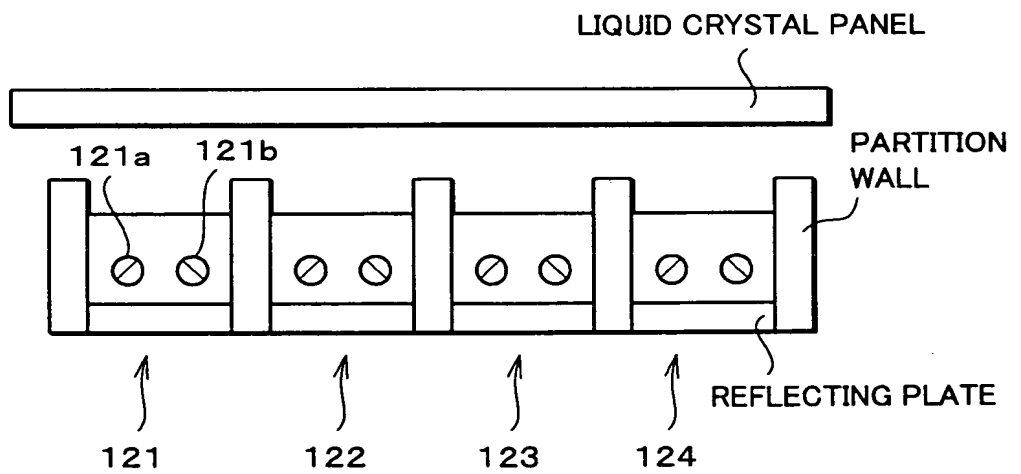


FIG. 23

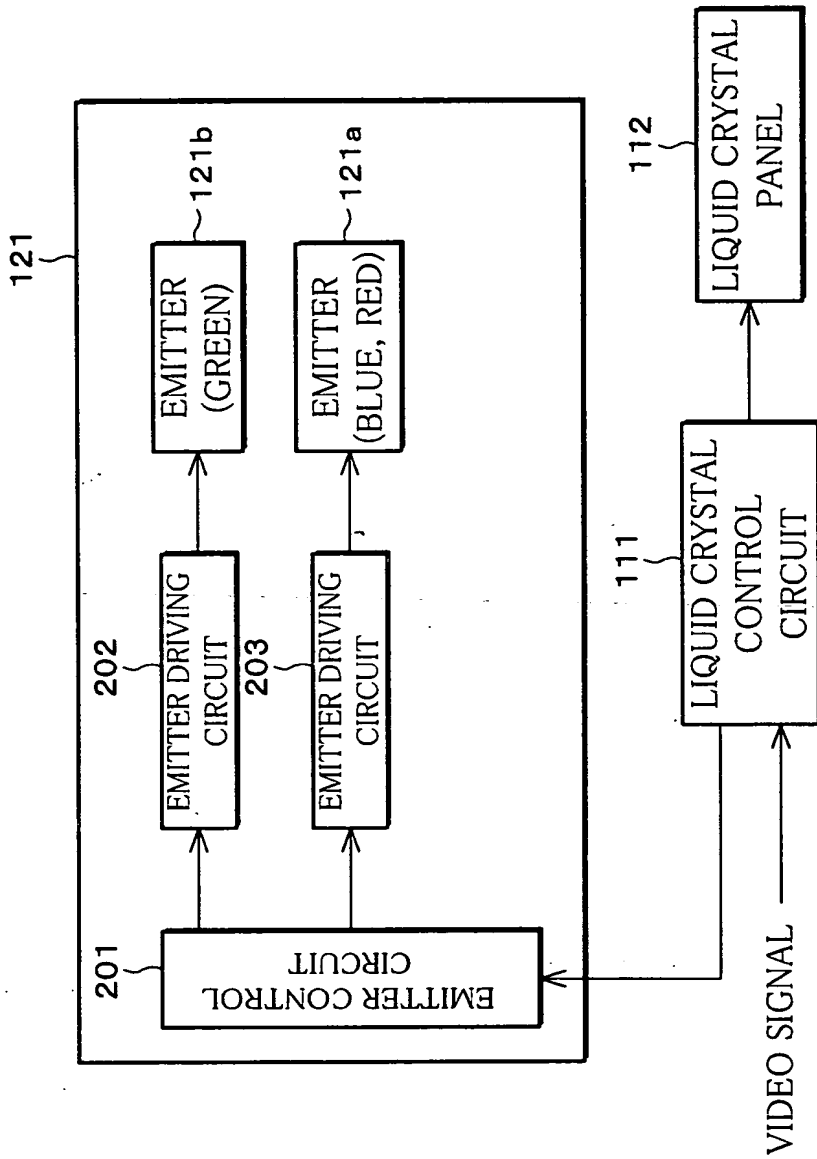
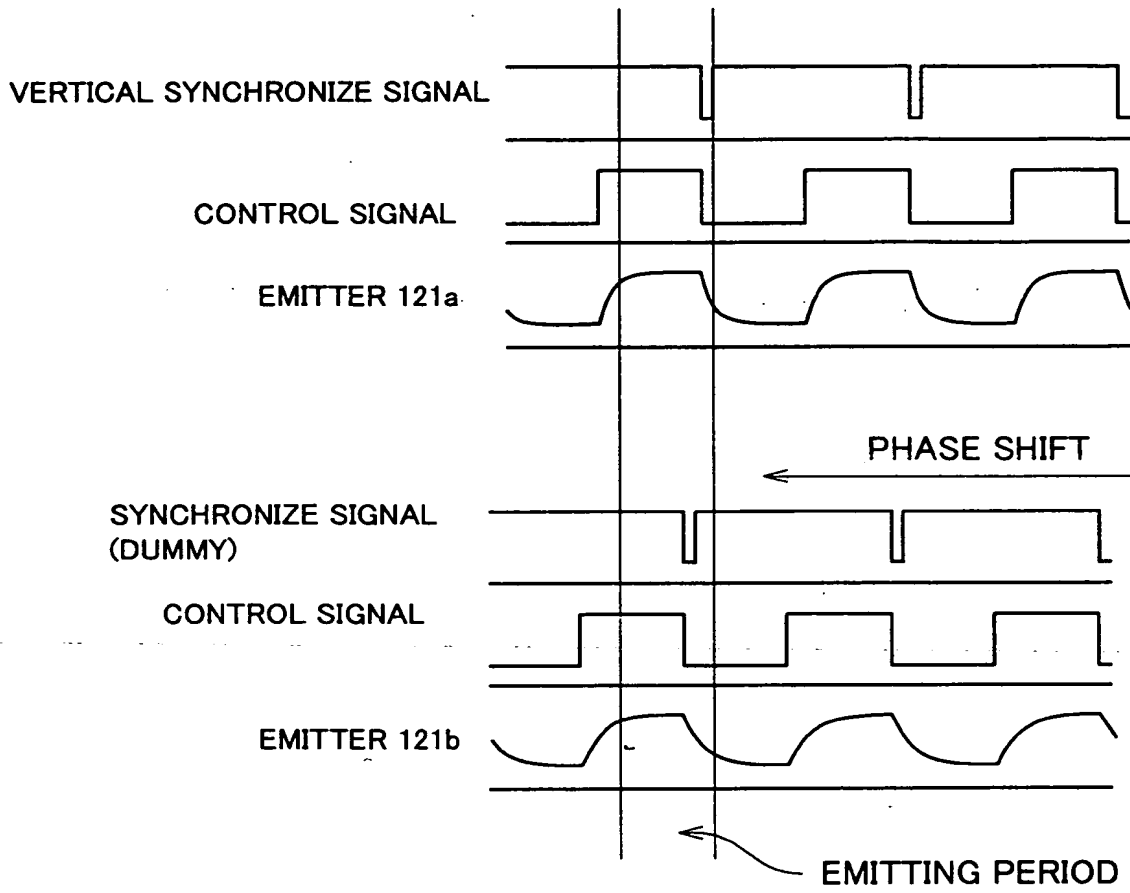


FIG. 24



TOP SECRET

FIG. 25

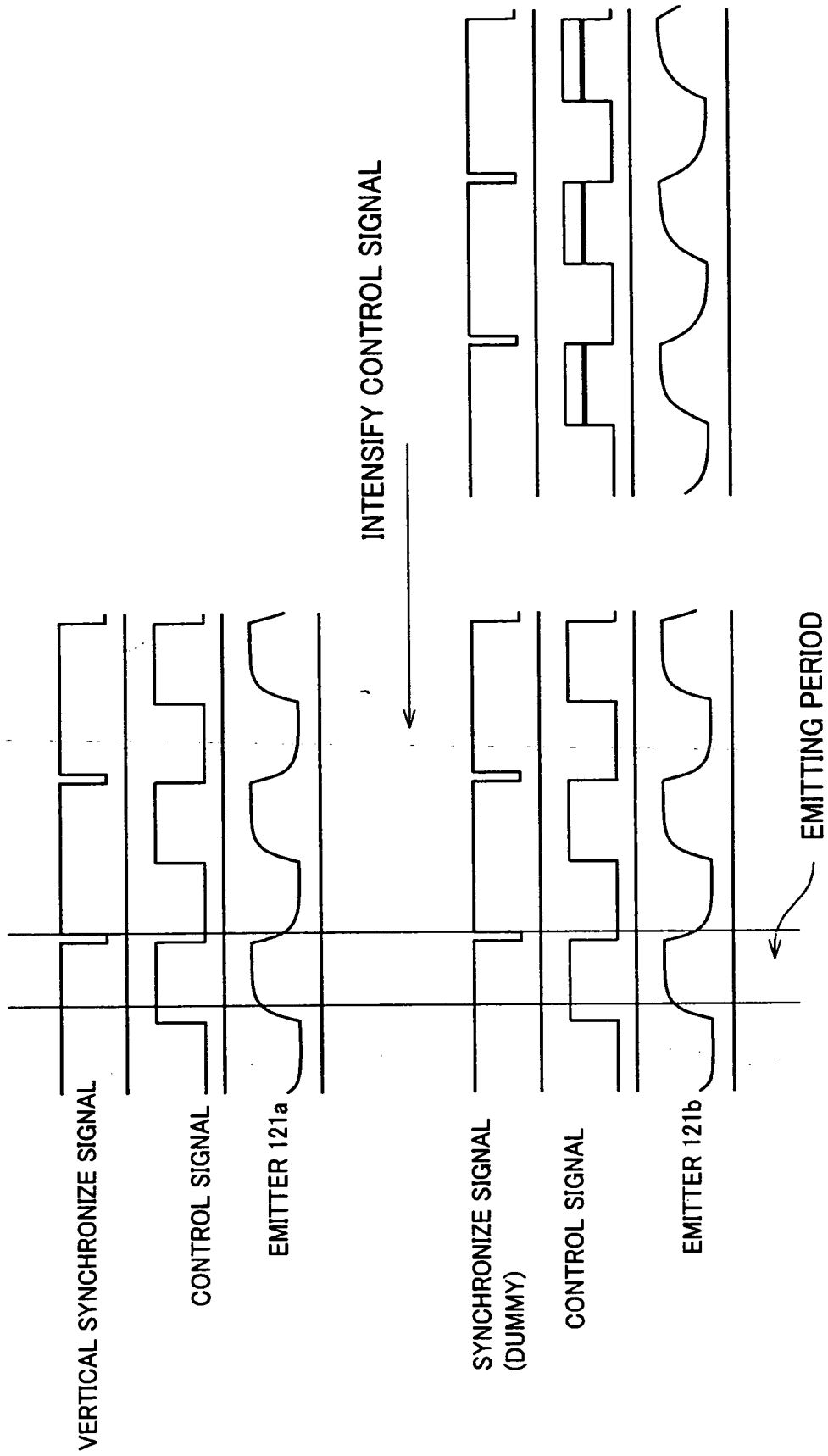


FIG. 26

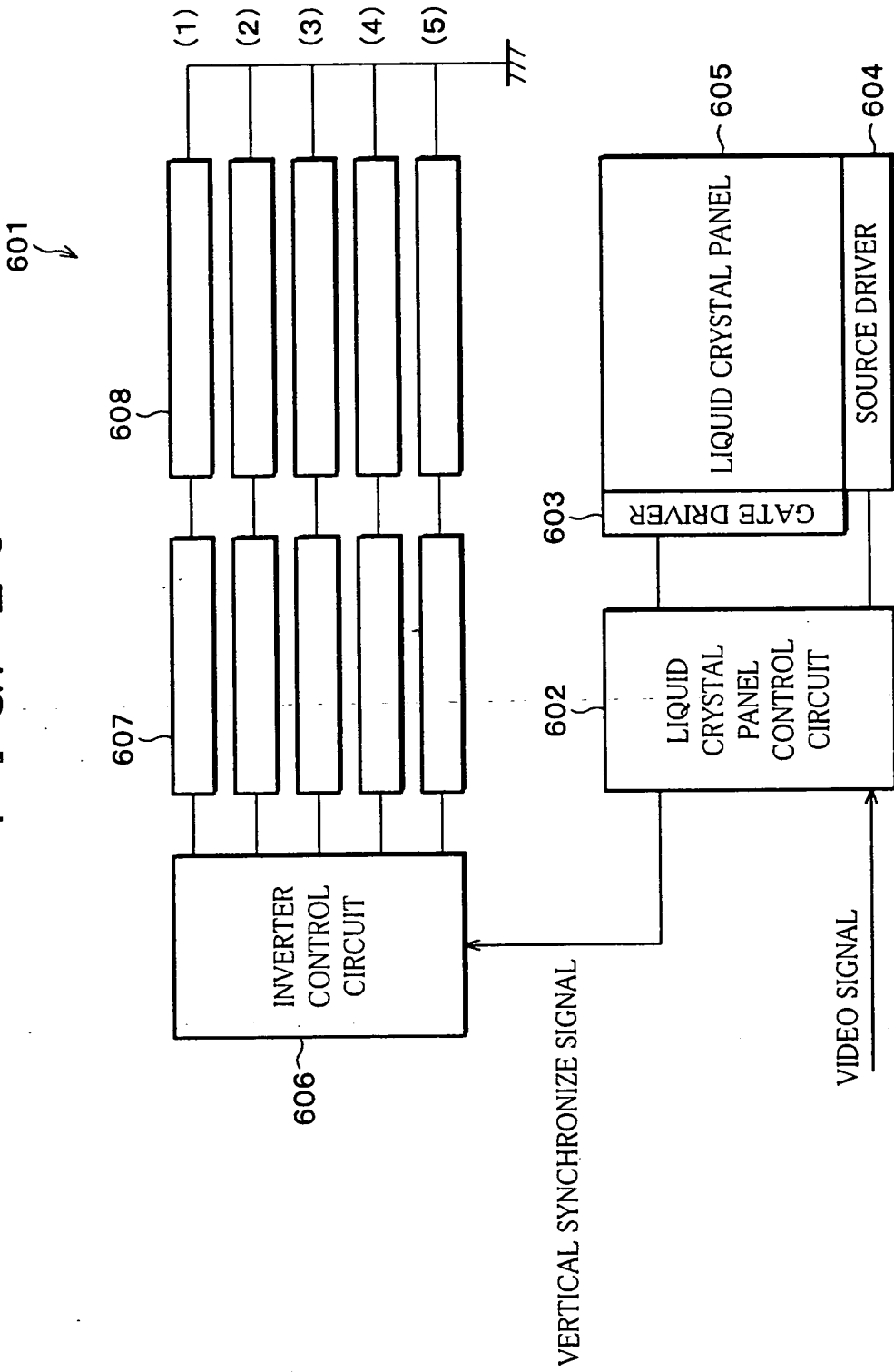
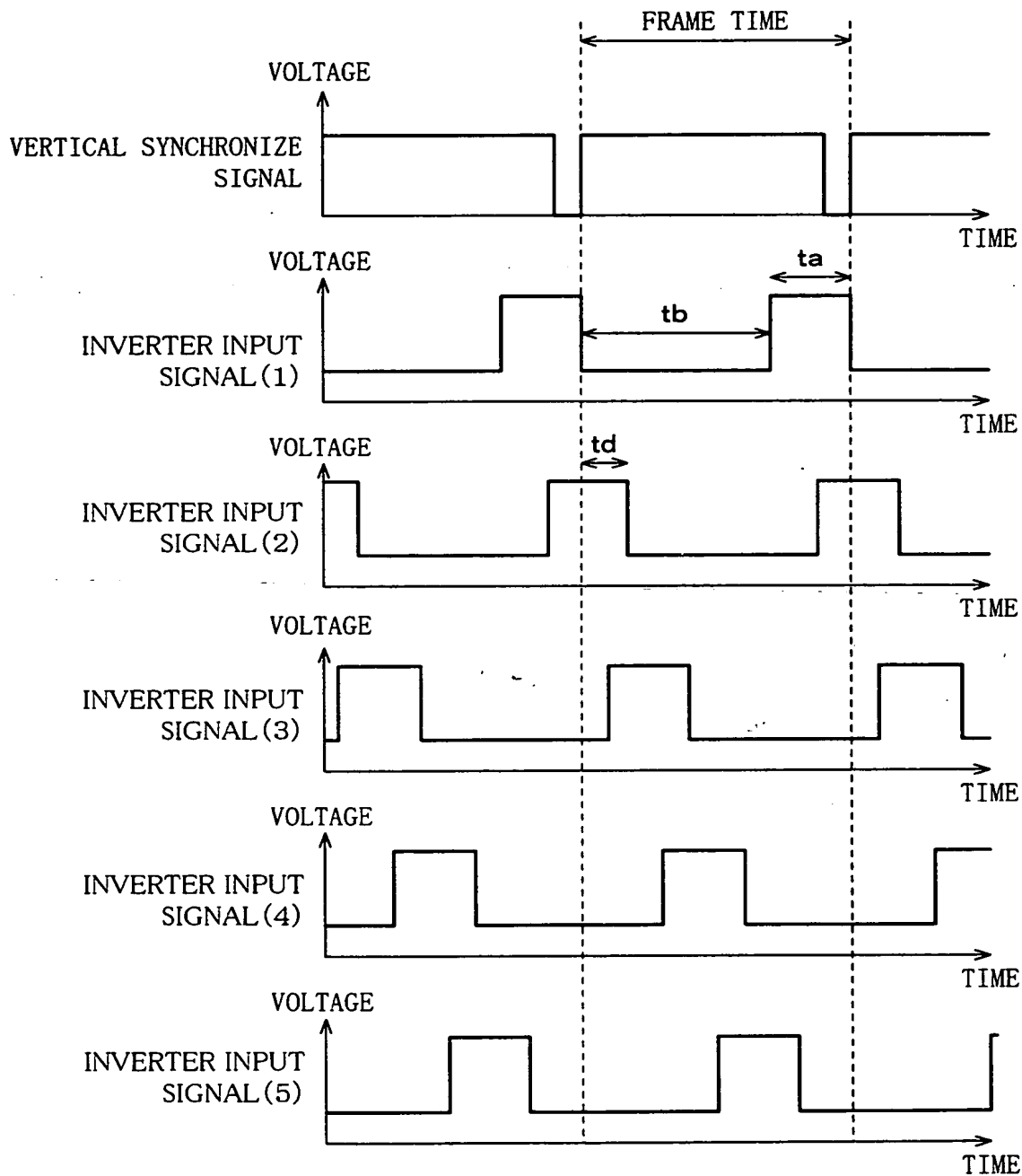


FIG. 27



TOP SECRET

FIG. 29

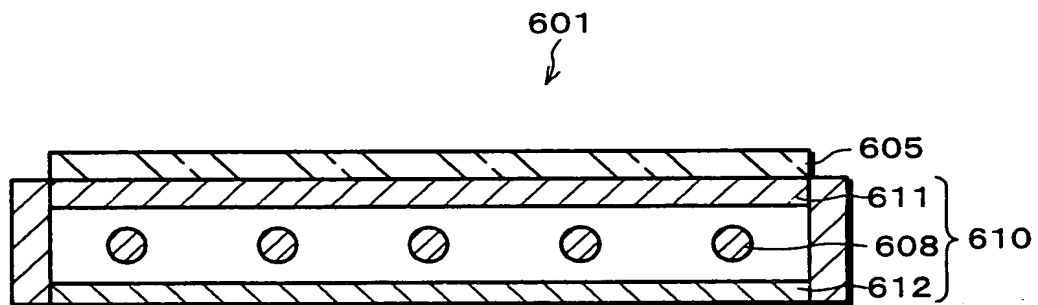


FIG. 30

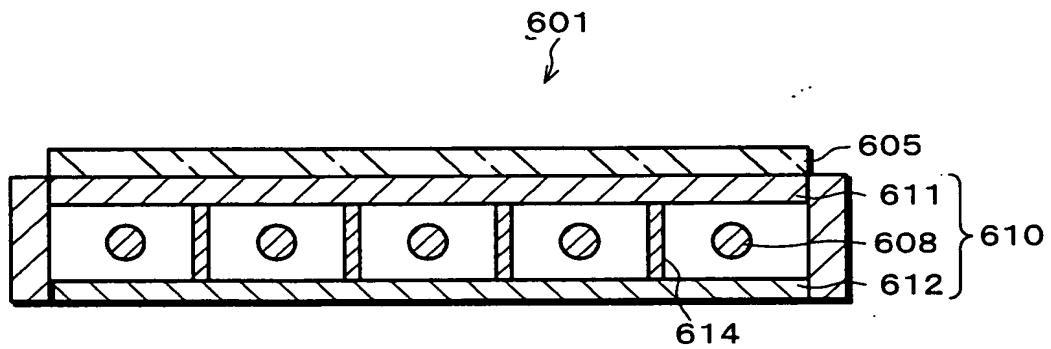


FIG. 30

FIG. 31

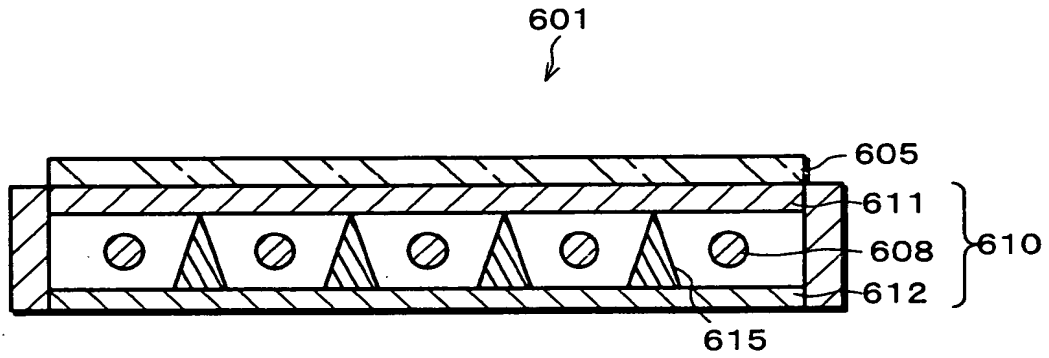


FIG. 32

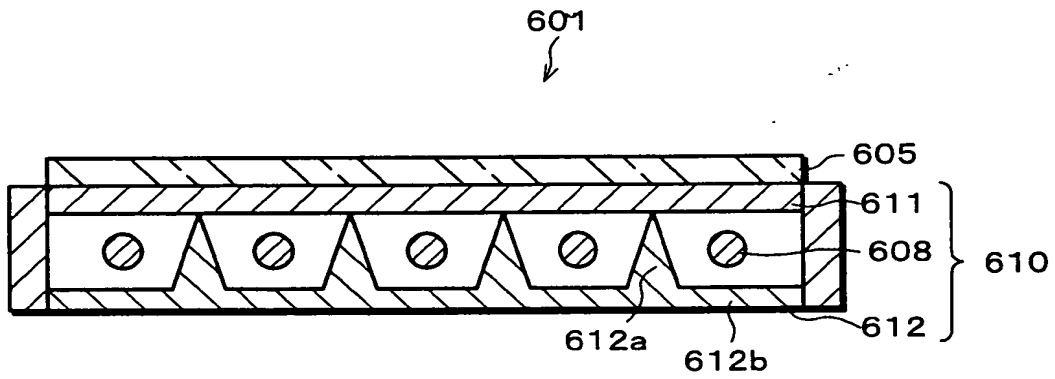


FIG. 31

FIG. 33

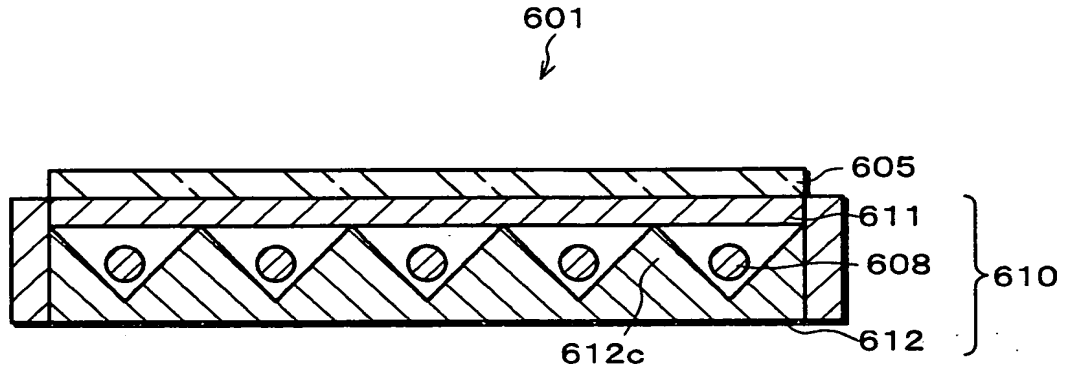
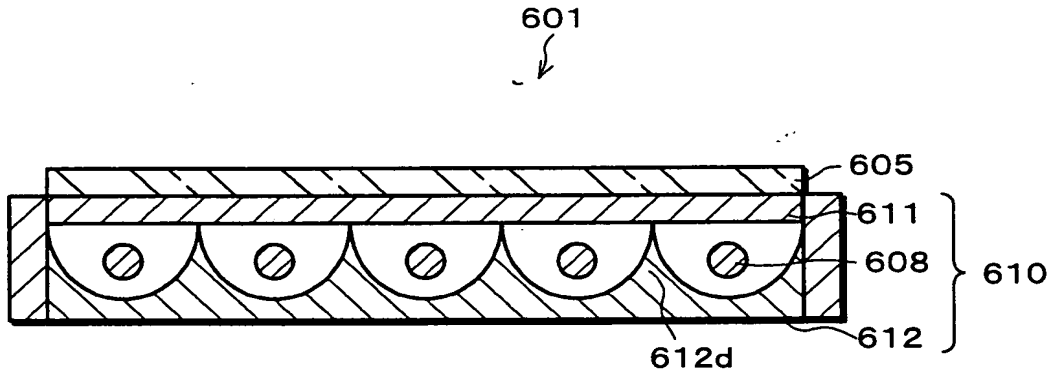


FIG. 34



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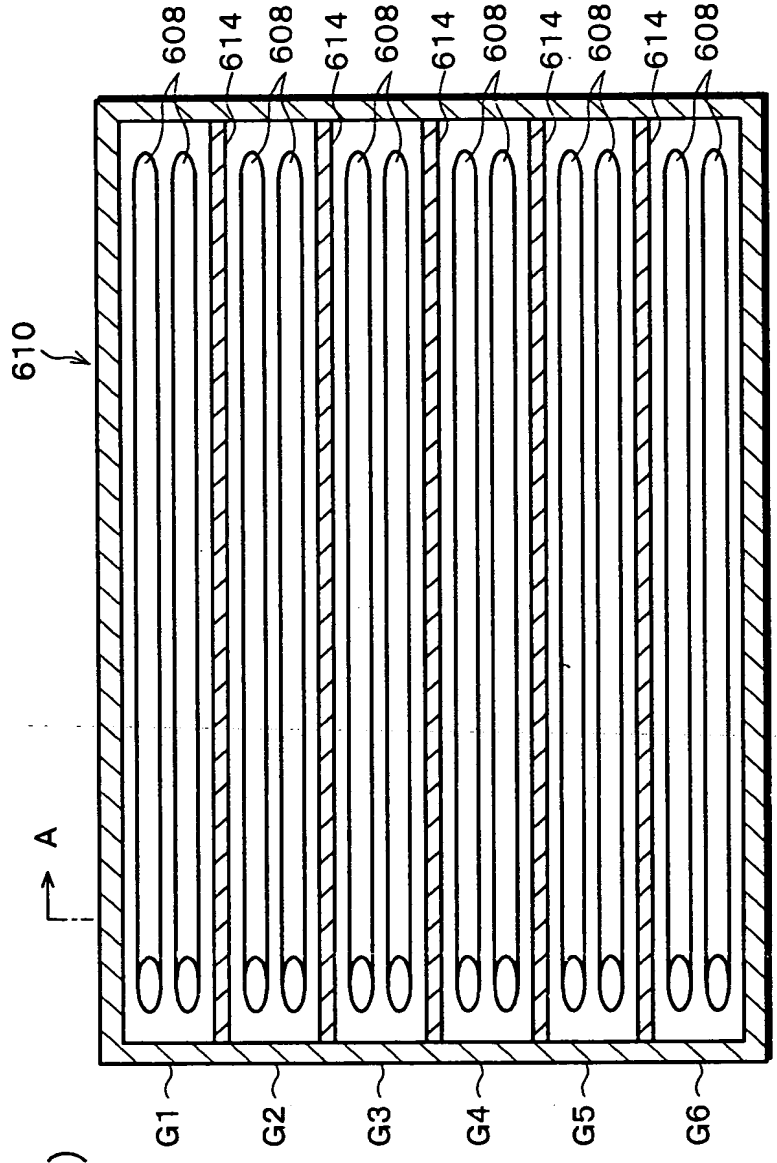


FIG. 35 (a)

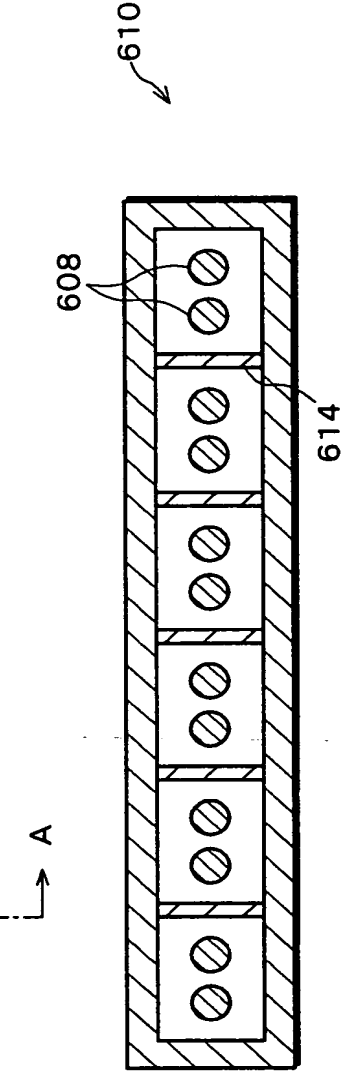


FIG. 35 (b)

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FIG. 36

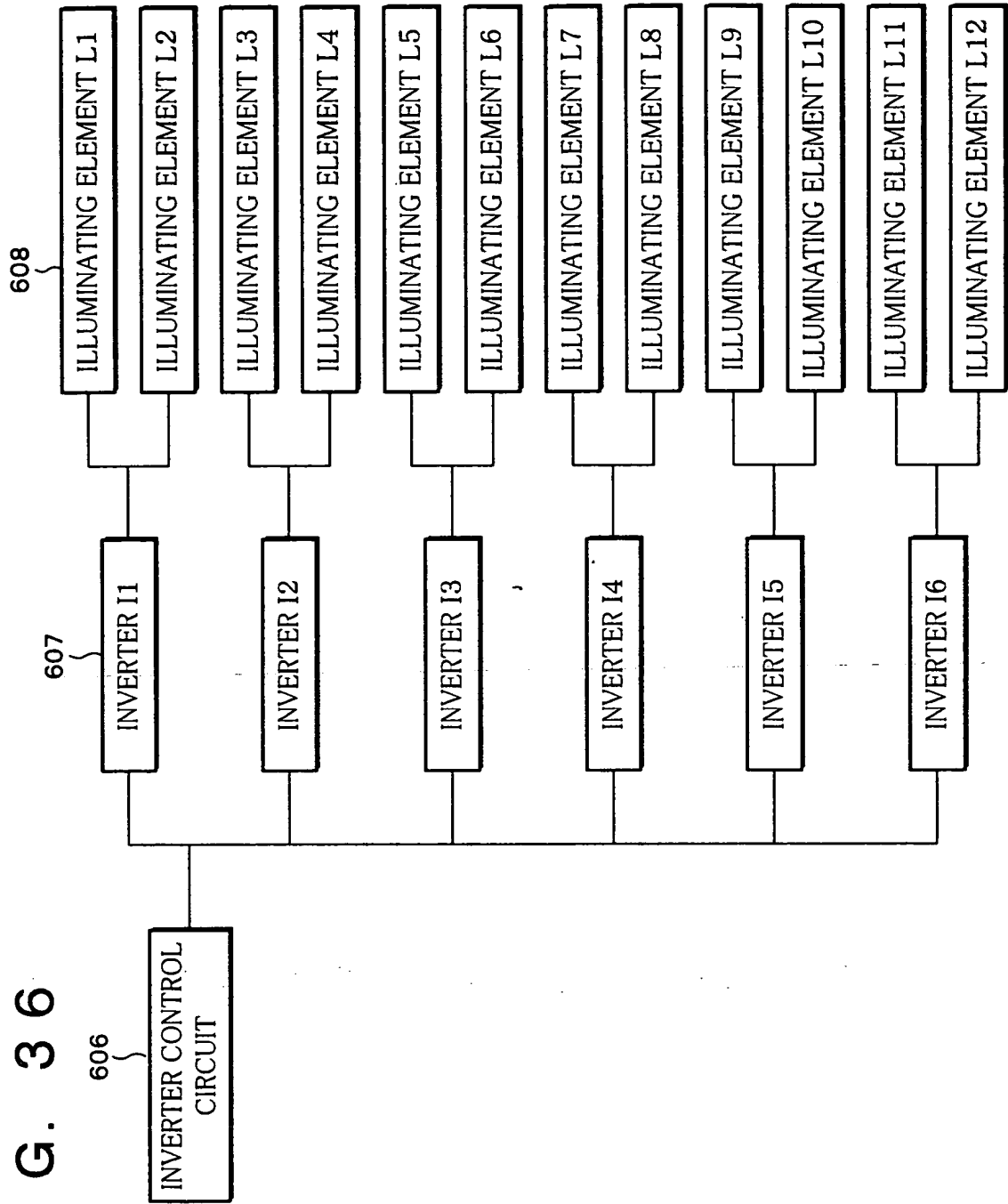


FIG. 37

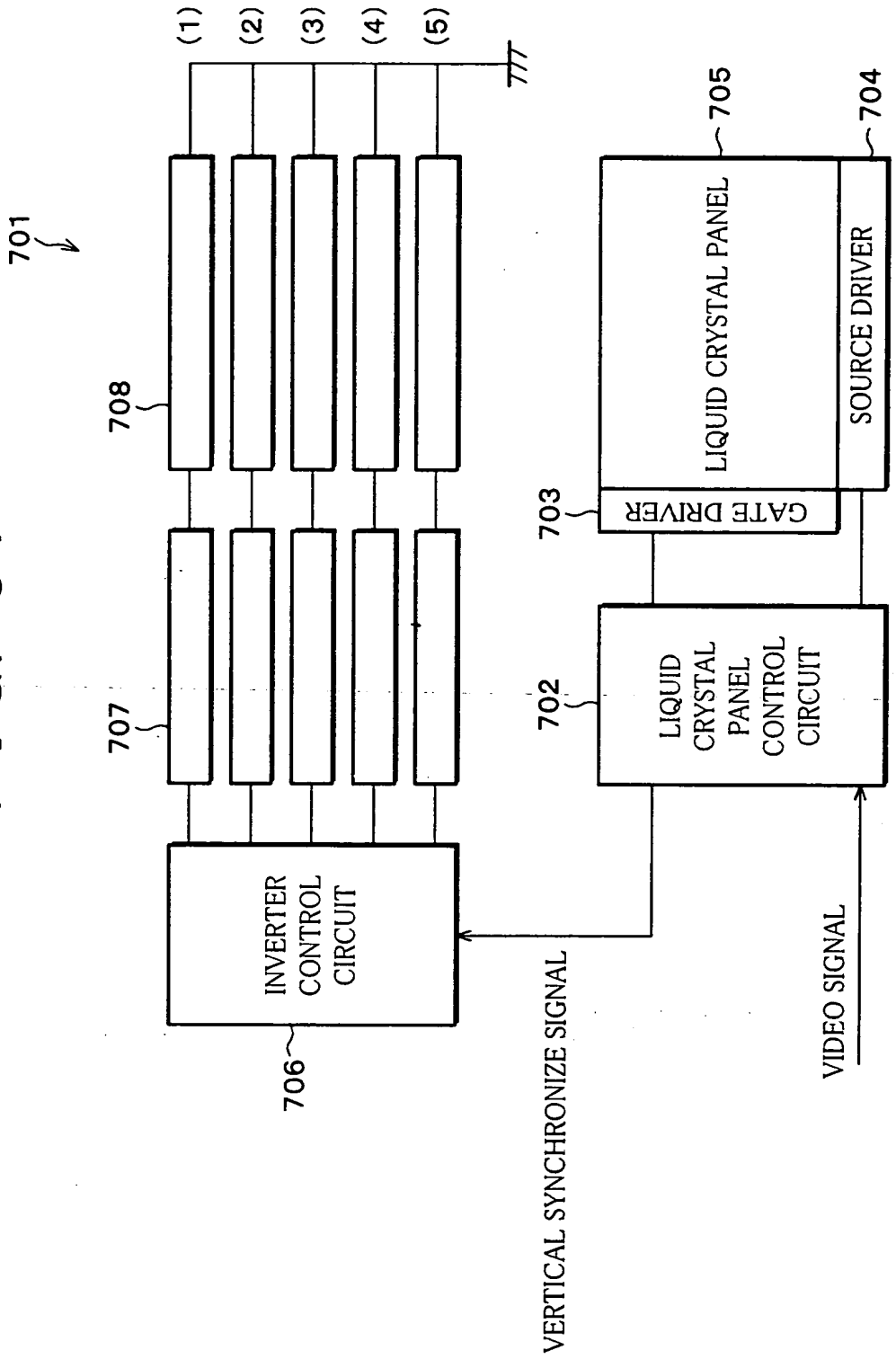
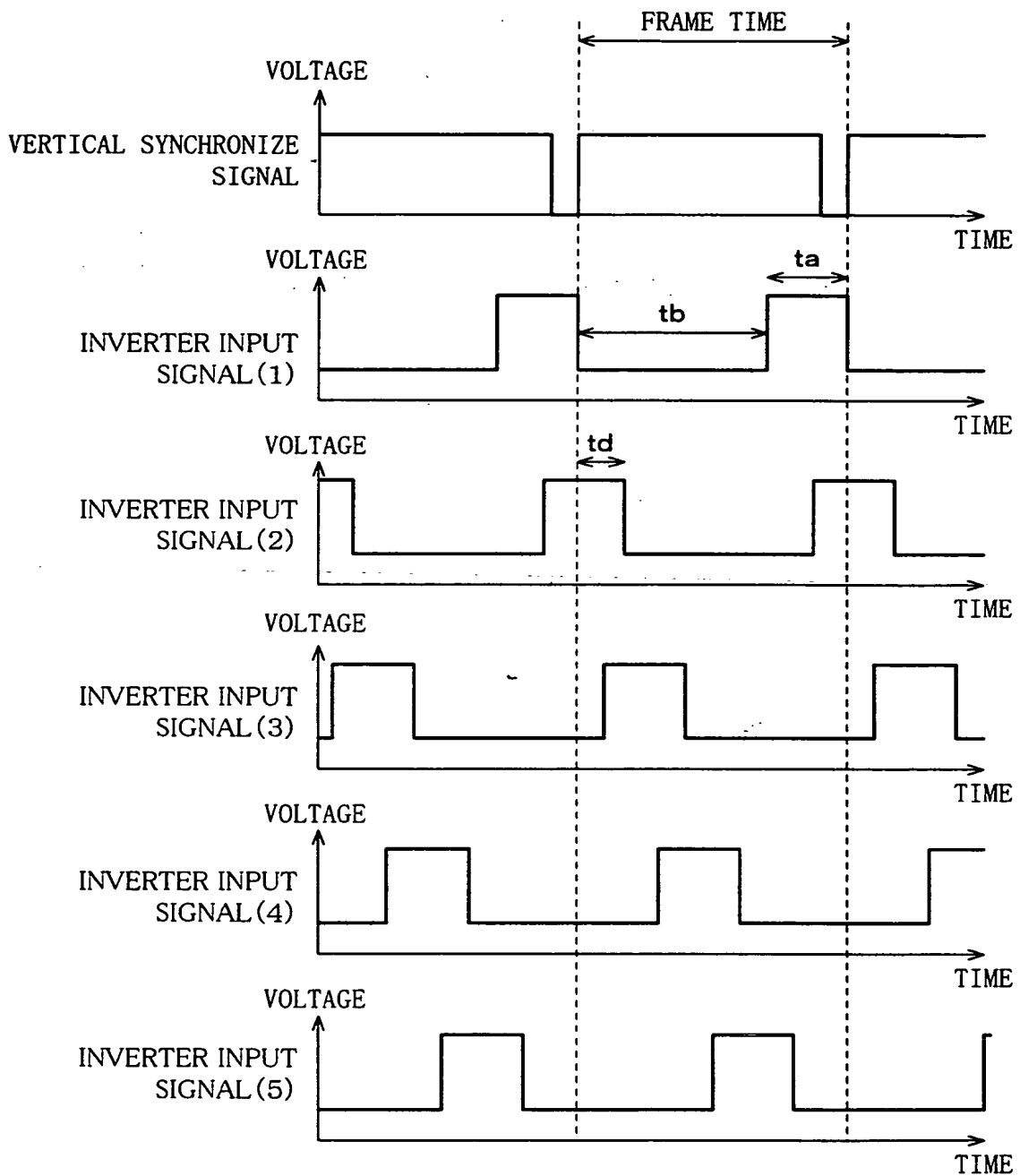
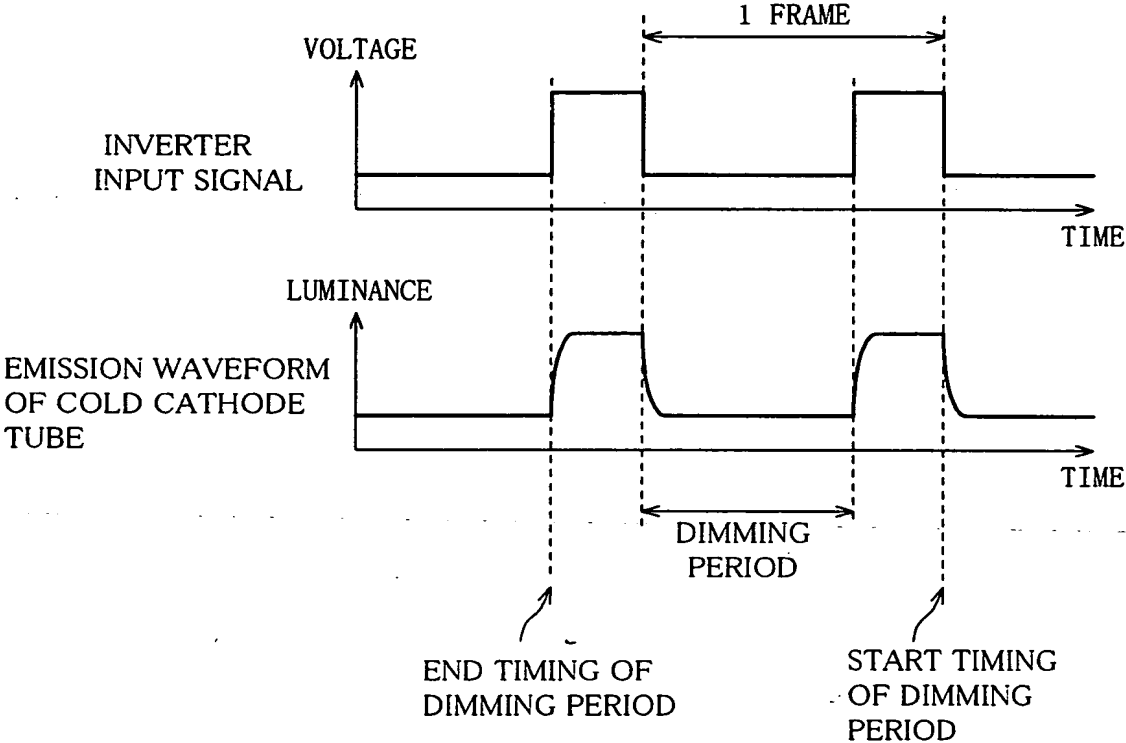


FIG. 38



FOOTNOTES

F I G. 3 9



14-00000-0000

FIG. 40

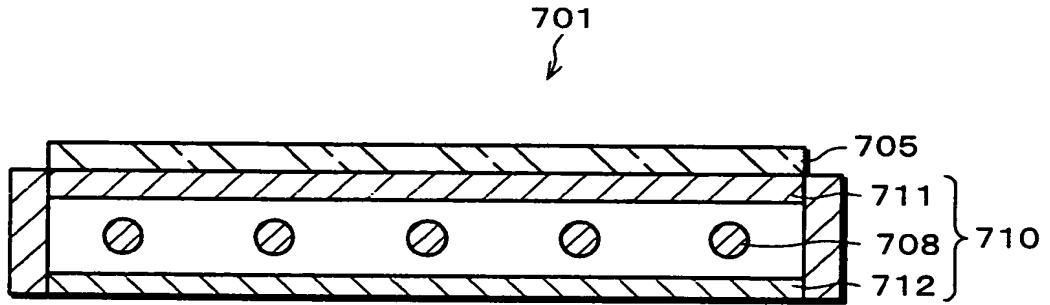


FIG. 40

FIG. 41

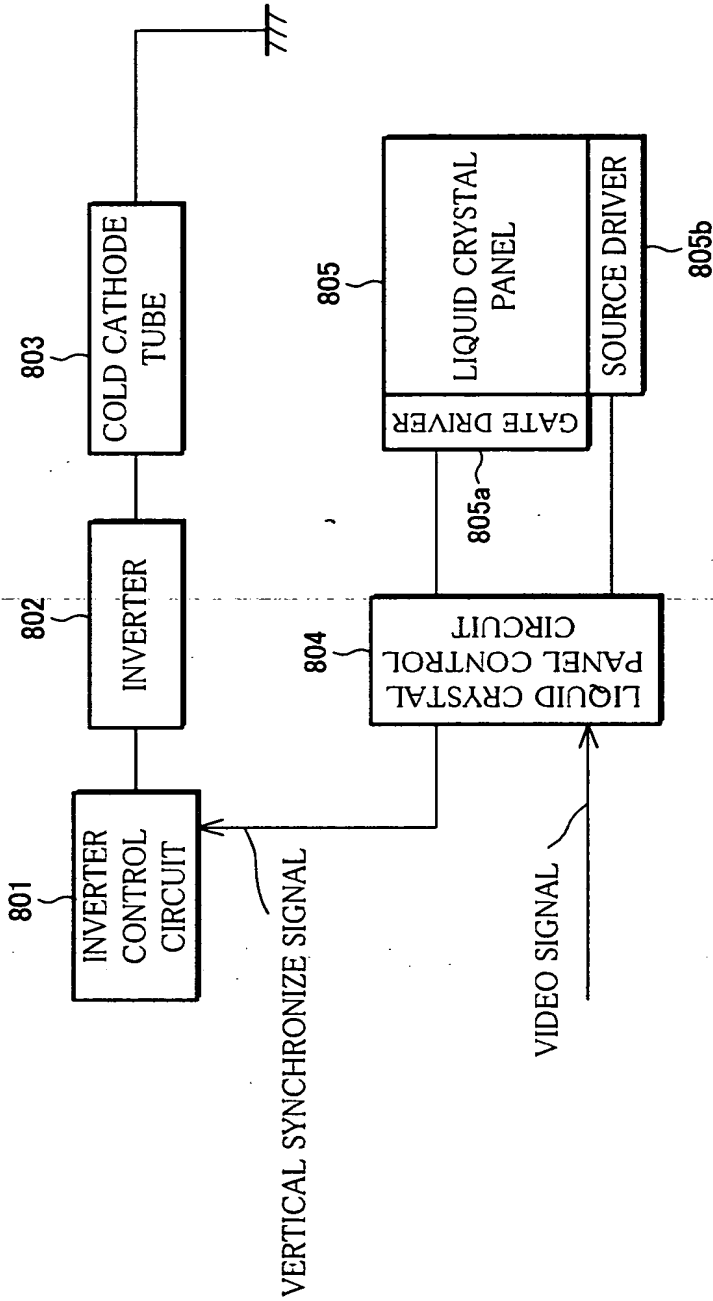
END TIMING OF DIMMING PERIOD

9/10	⊙	○	△	△	△	△	△	△	△	×
8/10	⊙	○	△	△	△	△	△	△	×	○
7/10	⊙	○	△	△	△	△	△	×	○	○
6/10	⊙	○	△	△	△	△	×	○	○	○
5/10	⊙	○	△	△	△	×	○	○	○	○
4/10	○	○	△	△	×	○	○	○	○	○
3/10	○	○	△	×	○	○	○	○	○	○
2/10	○	○	×	○	○	○	○	○	○	○
1/10	○	×	○	○	○	○	○	○	○	○
0/10	×	○	△	△	△	△	△	△	△	△
f	0/10	1/10	2/10	3/10	4/10	5/10	6/10	7/10	8/10	9/10

START TIMING OF DIMMING PERIOD

TABLE 100 - 10/10/10

FIG. 42



F I G. 4 3

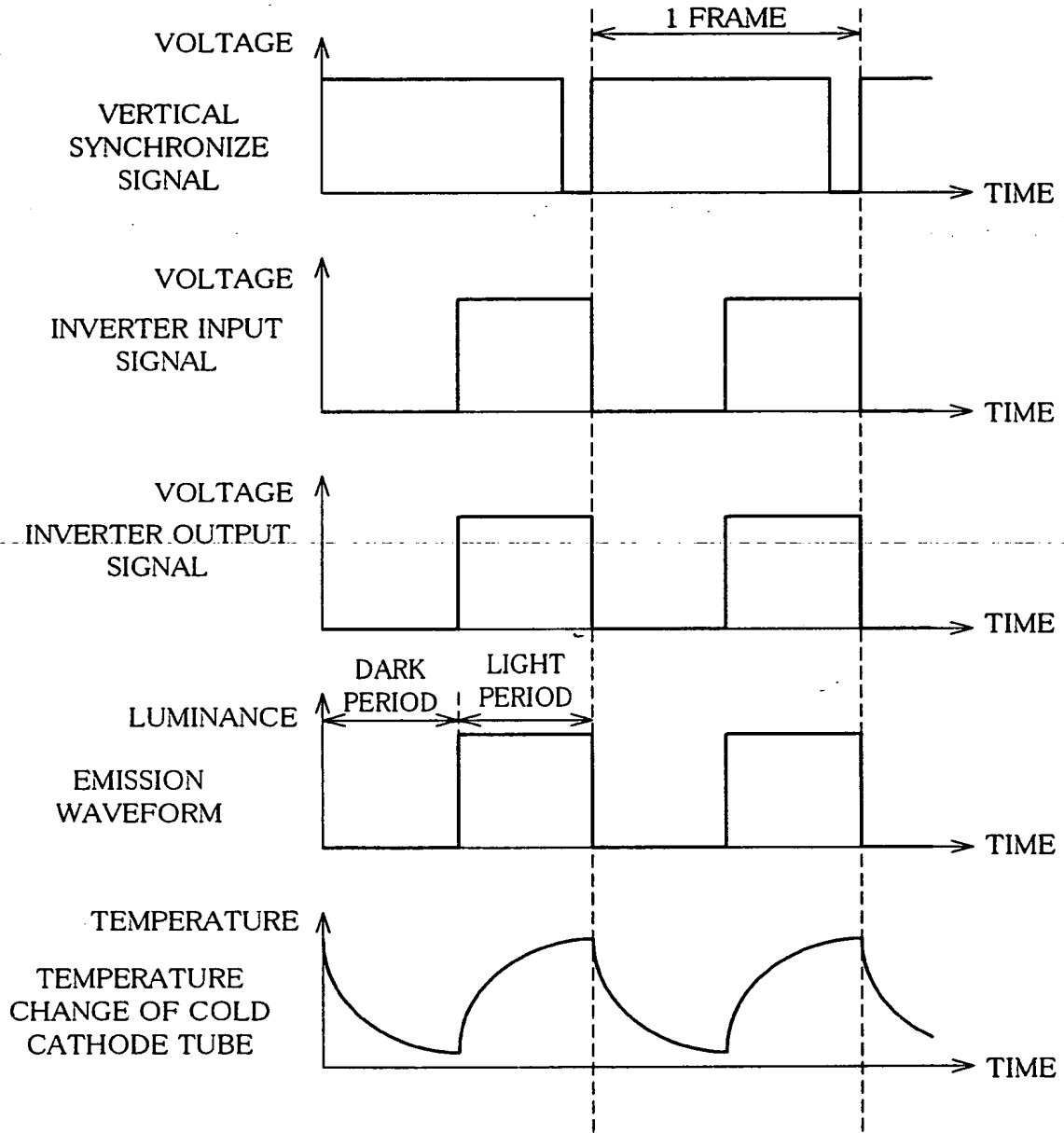
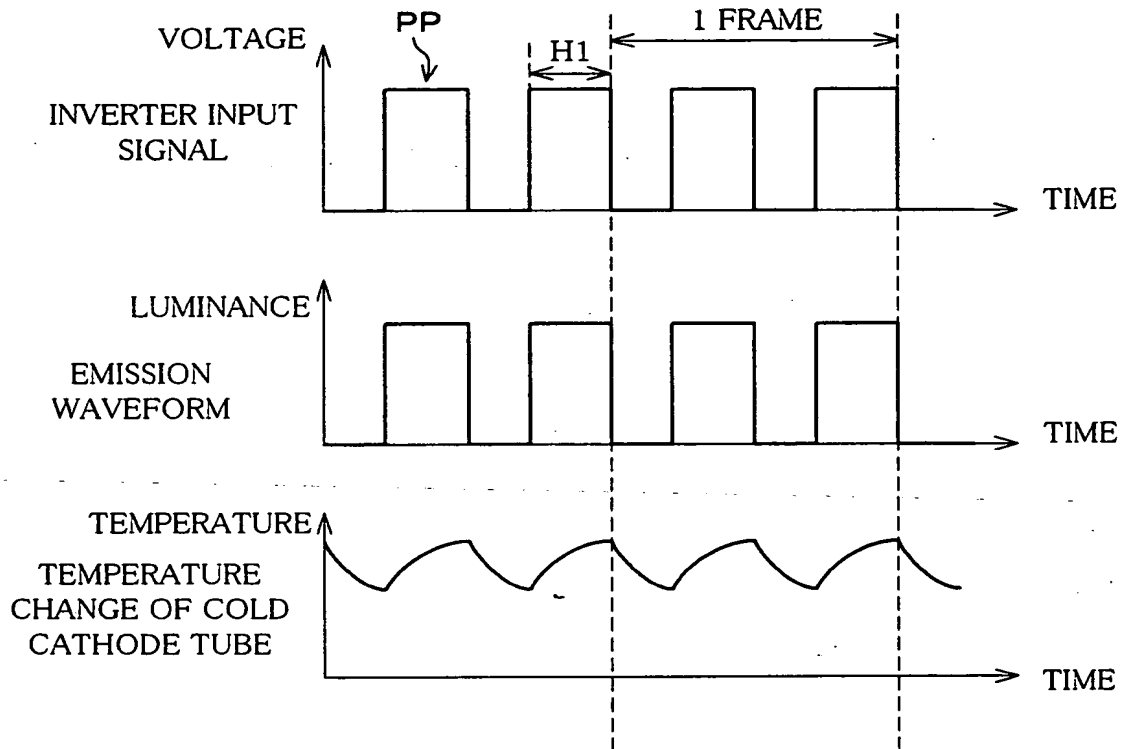


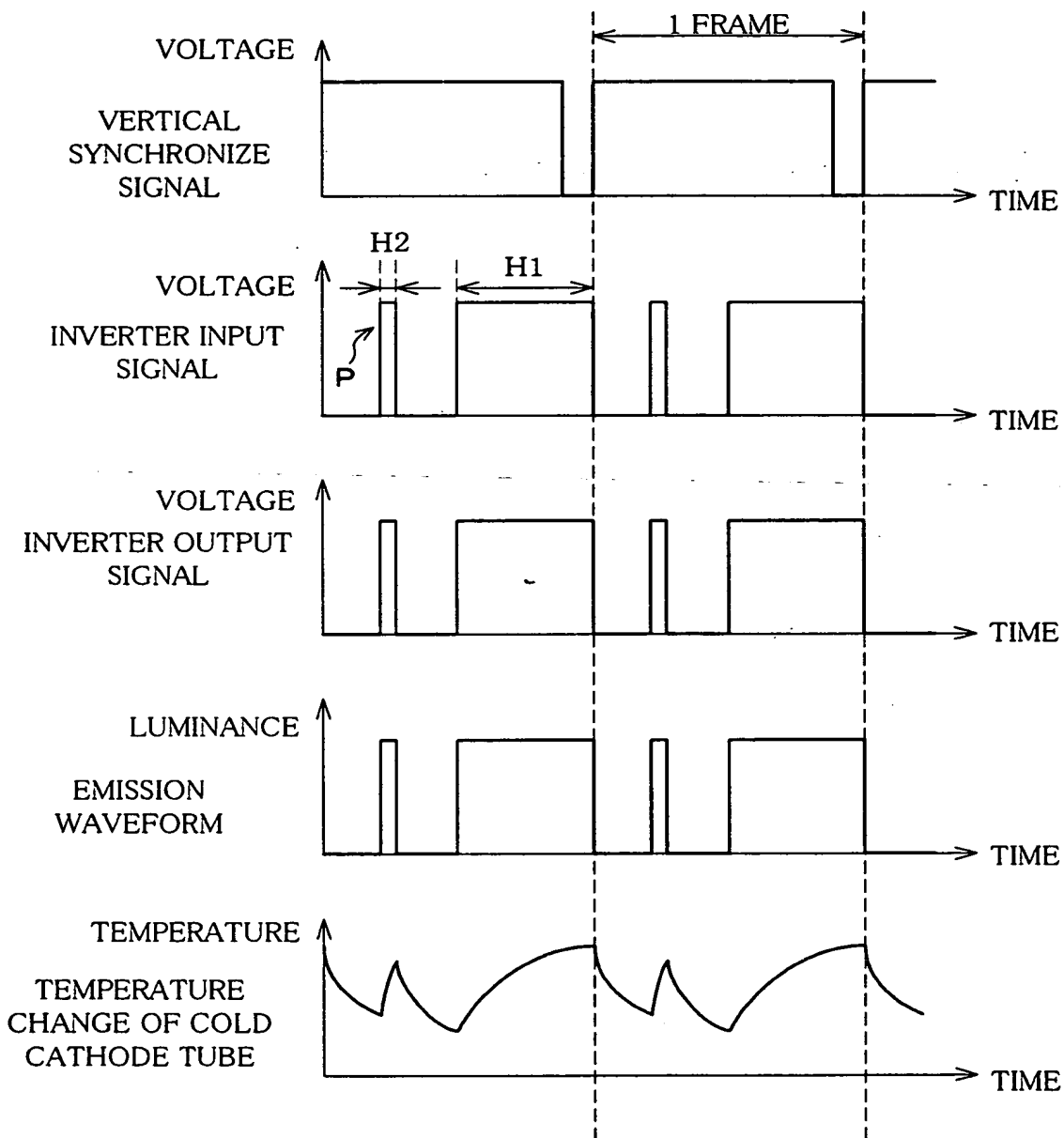
FIG. 43

FIG. 44



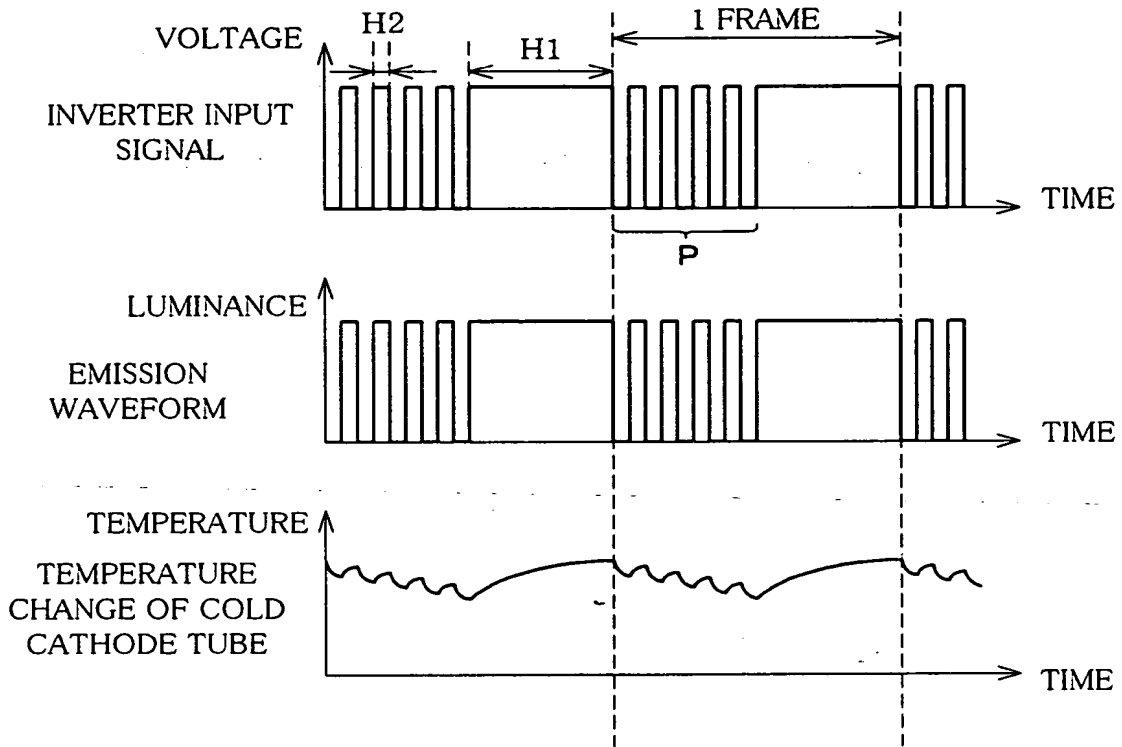
70750-536300

FIG. 45



TEFT30" 034300

FIG. 46



100-100000

FIG. 47

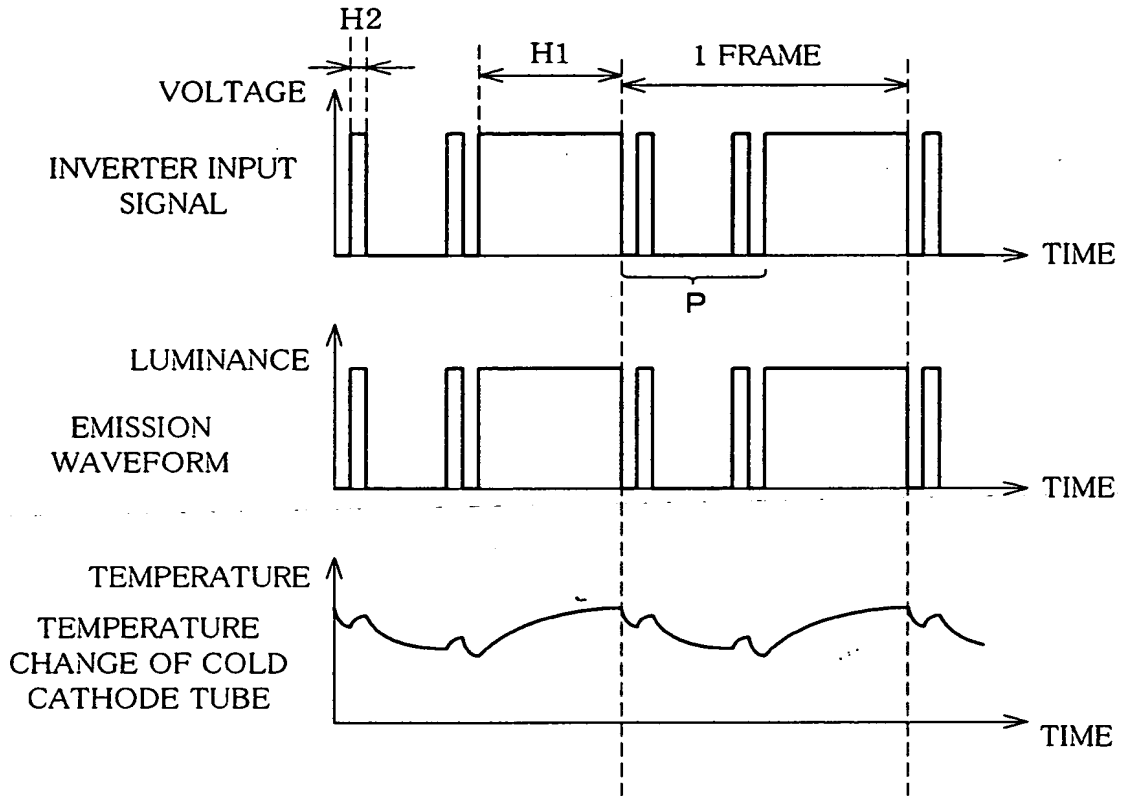
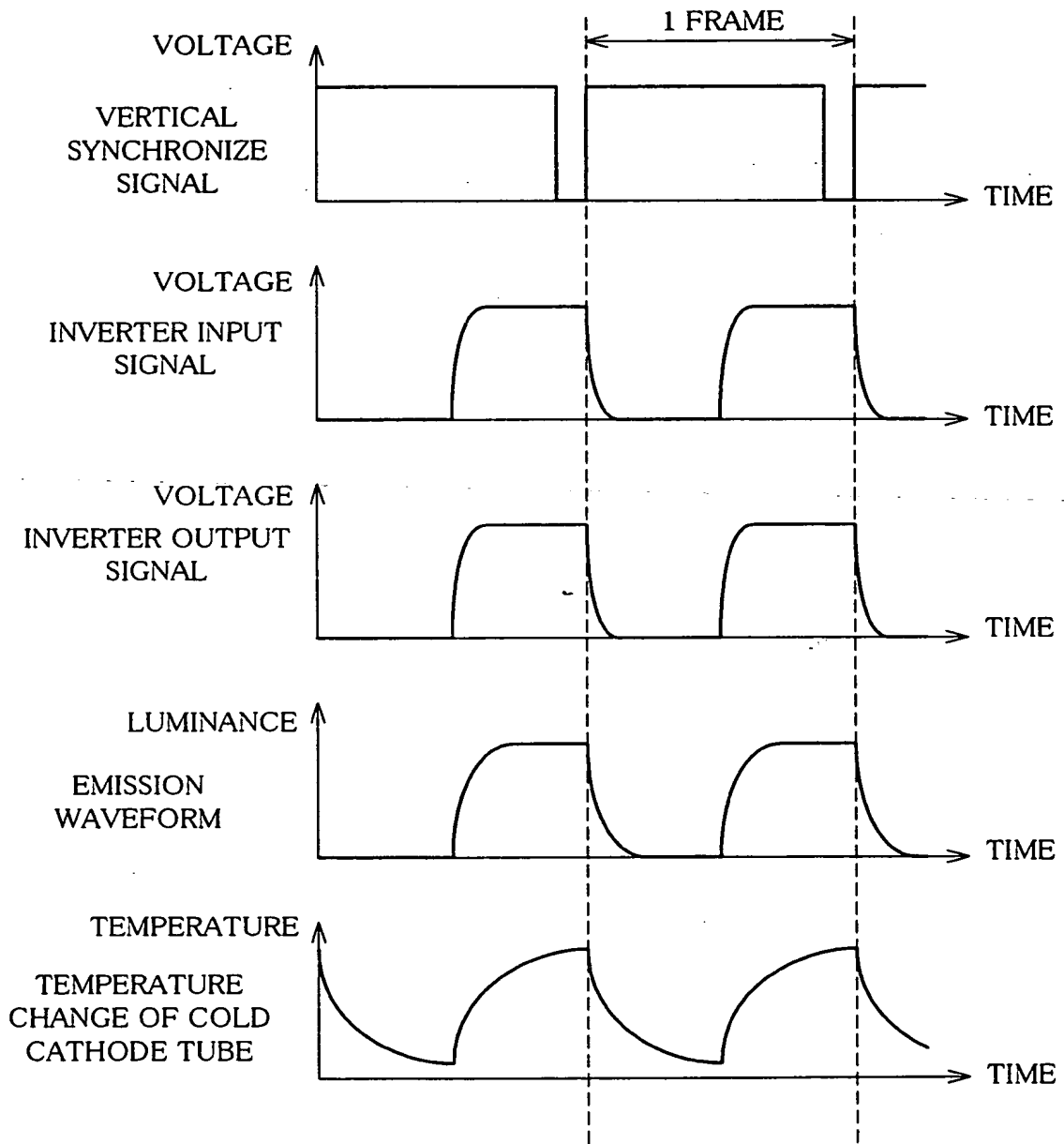


FIG. 47

FIG. 48



100-130-0000

FIG. 49

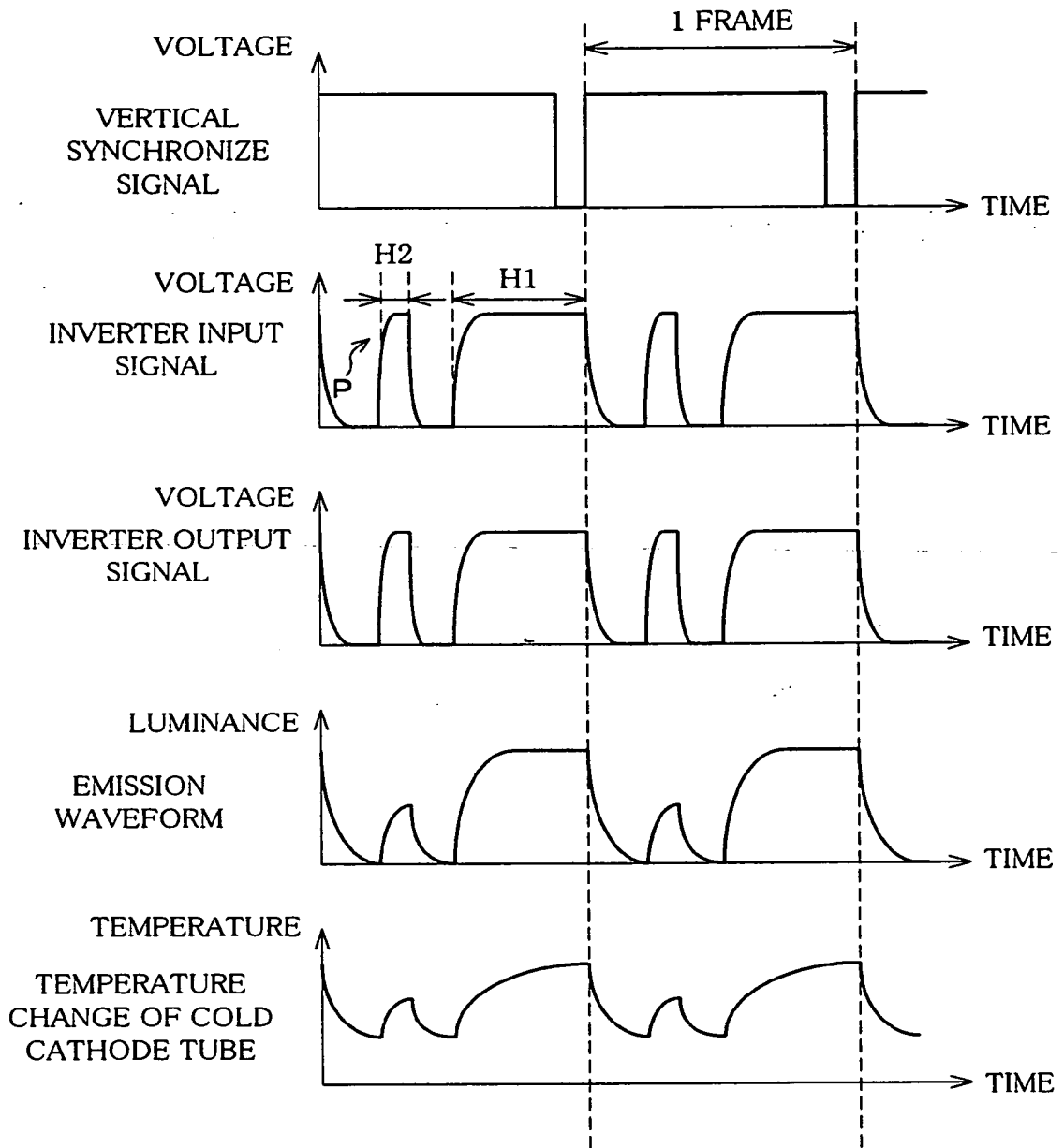


FIG. 49